

COMPAL CONFIDENTIAL

MODEL NAME : ZAM81
PCB NO : LA-A914P
BOM P/N :
GPIO MAP: 3.1

Huston 15" DSC Entry
Broadwell U

2013-08-20


REV : 0.1 (X00)

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- @ : Nopop Component
- EMC@ : EMI, ESD and RF Component
- @EMC@ : EMI, ESD and RF Nopop Component
- XDP@ : XDP Component
- CONN@ : Connector Component

MB PCB	
Part Number	Description
DA8000Z8000	PCB 13N LA-A914P RRV0 MB DSC NONDOCK 3

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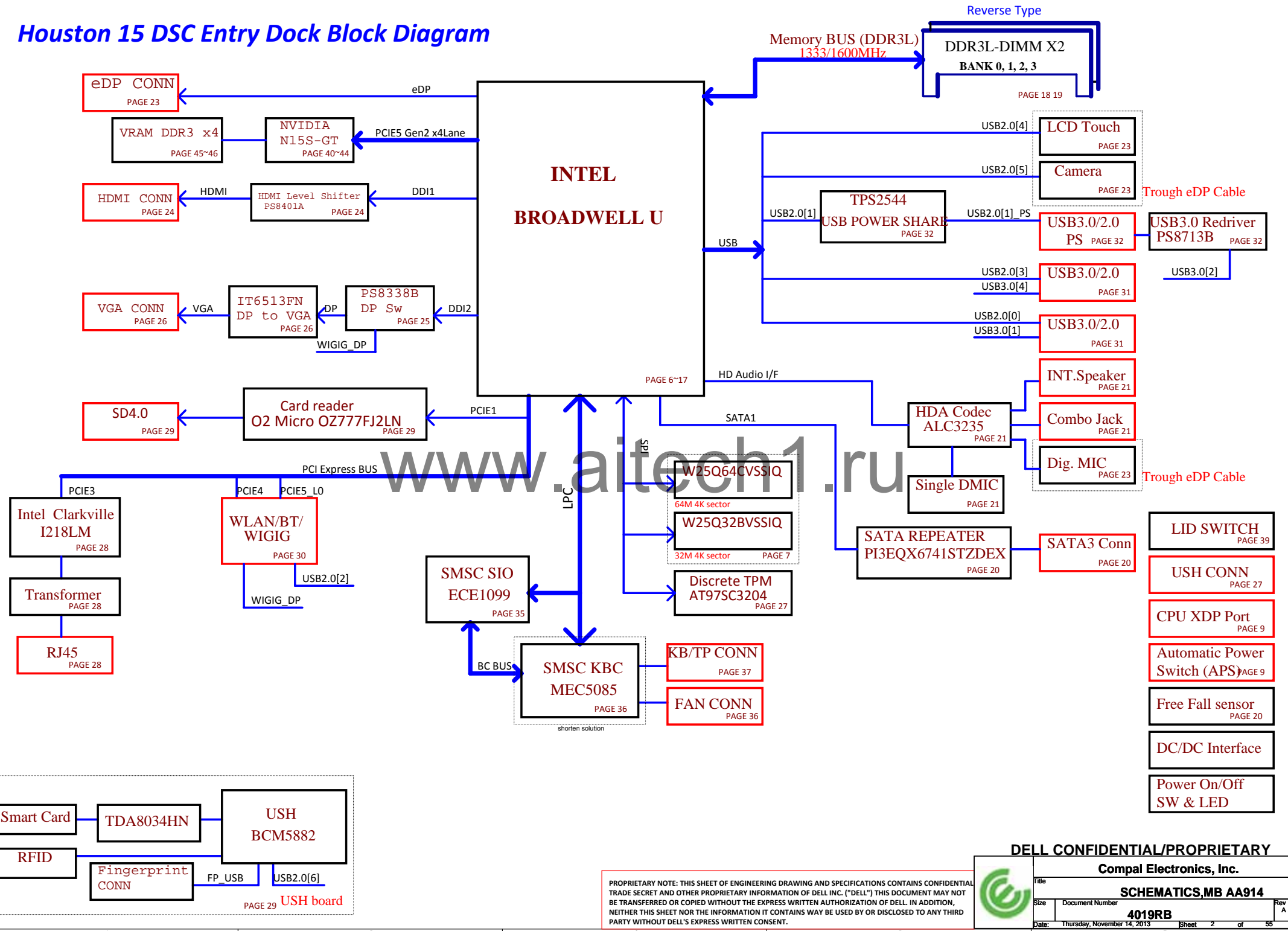
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Title: **SCHEMATICS,AA914 ZAM81**

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Houston 15 DSC Entry Dock Block Diagram



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POWER STATES

Signal State	SLP S3#	SLP S4#	SLP S5#	SLP A#	ALWAYS PLANE	M PLANE	SUS PLANE	RUN PLANE	CLOCKS
S0 (Full ON) / M0	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON	ON
S3 (Suspend to RAM) / M3	LOW	HIGH	HIGH	HIGH	ON	ON	ON	OFF	OFF
S4 (Suspend to DISK) / M3	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF	OFF
S5 (SOFT OFF) / M3	LOW	LOW	LOW	HIGH	ON	ON	OFF	OFF	OFF
S3 (Suspend to RAM) / M-OFF	LOW	HIGH	HIGH	LOW	ON	OFF	ON	OFF	OFF
S4 (Suspend to DISK) / M-OFF	LOW	LOW	HIGH	LOW	ON	OFF	OFF	OFF	OFF
S5 (SOFT OFF) / M-OFF	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF	OFF

PM TABLE

power plane State	+5V_ALW +3.3V_ALW +3.3V_ALW_PCH +3.3V_RTC_LDO	+3.3V_SUS +1.35V_MEM	+5V_RUN +3.3V_RUN +0.675V_DDR_VTT +1.05V_RUN +VCC_CORE	+3.3V_M +1.05V_M	+3.3V_M +1.05V_M (M-OFF)
S0	ON	ON	ON	ON	ON
S3	ON	ON	OFF	ON	OFF
S5 S4/AC	ON	OFF	OFF	ON	OFF
S5 S4/AC doesn't exist	OFF	OFF	OFF	OFF	OFF

need to update Power Status and
PM Table

PCIE	USB3.0	SATA	DESTINATION
	USB3.0 1		JUSB1-->Rear left
	USB3.0 2		JUSB3-->Right
PCIE 1	USB3.0 3		MMI (CARD READER)
PCIE 2	USB3.0 4		JUSB2-->Rear Right
PCIE 3			LOM
PCIE 4			WLAN
PCIE 5			GPU/WIGIG
PCIE 6		SATA 3	WIGI/Express
		SATA 2	mSATA/PCIE
		SATA 1	HDD
		SATA 0	DOCK

USB PORT#	DESTINATION
0	JUSB1
1	JUSB3
2	WLAN + BT
3	JUSB2
4	Touch Screen
5	CAMERA
6	USH
7	WWAN

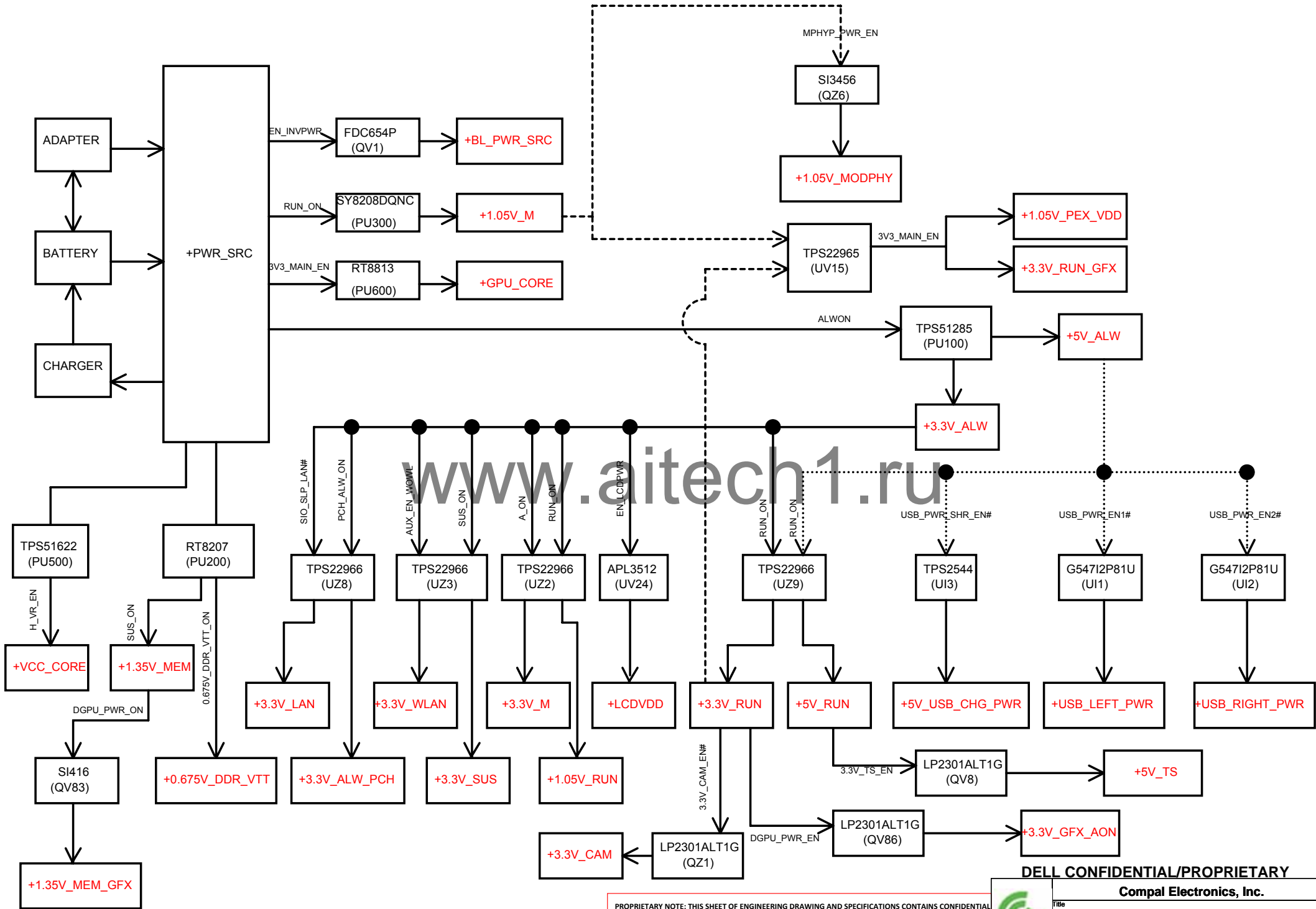
USH	0	BIO
	1	NA

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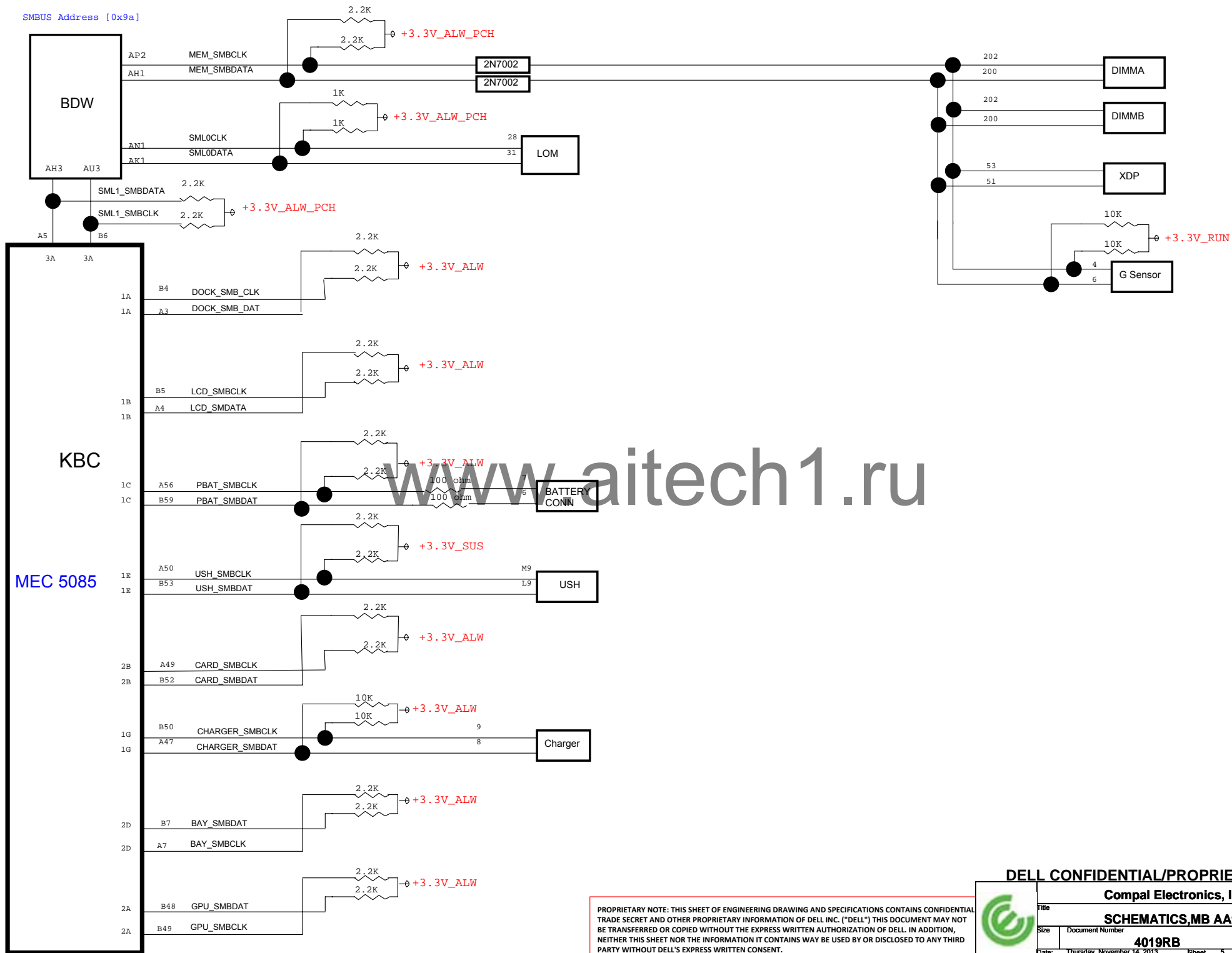
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SMBUS Address [0x9a]



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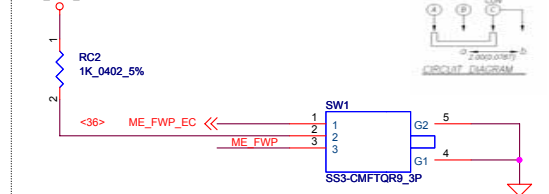
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DSC SATA port

Service Mode Switch:

Add a switch to ME_FWP signal to unlock the ME region and allow the entire region of the SPI flash to be updated using FPT.

+3.3V_ALW_PCH

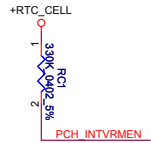


ME_FWP PCH has internal 20K PD.

FLASH DESCRIPTOR SECURITY OVERRIDE

ME_FWP=LOW → ENABLE ME (DEFAULT) → Pin1 & Pin3 short

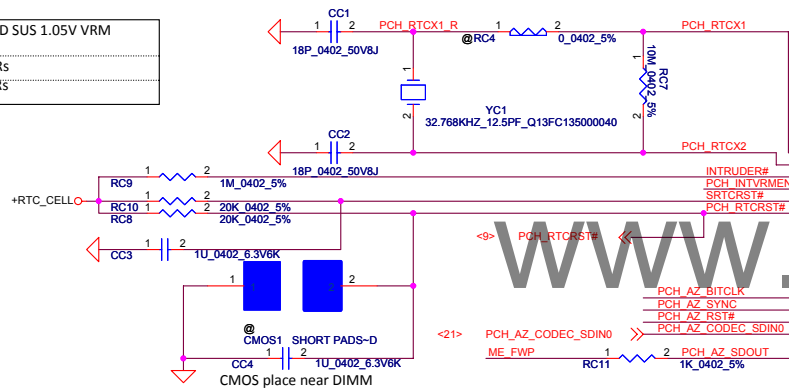
=HIGH → DISABLE ME (ME can update) → Pin2 & Pin3 short



INTVRMEN - INTEGRATED SUS 1.05V VRM
ENABLE

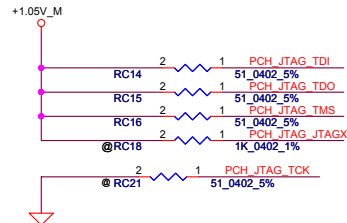
High - Enable Internal VRs

Low - Enable External VRs

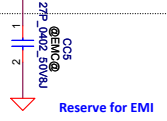
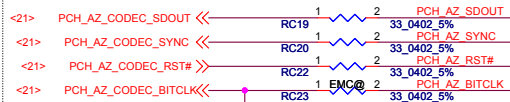


ME_CLR1	TPM setting
Shunt	Clear ME RTC Registers
Open	Keep ME RTC Registers

CMOS_CLR1	CMOS setting
Shunt	Clear CMOS
Open	Keep CMOS



HDA for Codec



SATA0	SATA1	PCB	SATA2/PCIE6 L1	SATA3/PCIE6 L0
E-Dock	HDD	H12 UMA	M2 3042 2nd PCIe Lane for PCIe Cache	M2 3042 (HCA & SATA-Cache)
NA	HDD	H12 Entry	NA	NA
E-Dock	HDD	H14 DSC	M2 3042 SATA-Cache(no HCA)	M2 3030 WIGIG
E-Dock	HDD	H14 UMA	M2 3042 2nd PCIe Lane for PCIe Cache	M2 3042 (HCA & SATA-Cache)
NA	HDD	H14D_En	NA	M2 3030 WIGIG
NA	HDD	H14U_En	NA	NA
E-Dock	HDD	H15 DSC	M2 3042 SATA-Cache(no HCA)	M2 3030 WIGIG
E-Dock	HDD	H15 UMA	M2 3042 2nd PCIe Lane for PCIe Cache	M2 3042 (HCA & SATA-Cache)
NA	HDD	H15D_En	NA	M2 3030 WIGIG
NA	HDD	H15U_En	NA	Express card

contact to WWAN

SATA2/PCIE6_L1 contact to WWAN
SATA3/PCIE6 L0 contact to WLAN

contact to WWAN

contact to WLAN

SATA2/PCIE6_L1 contact to WWAN
SATA3/PCIE6 L0 contact to WLAN

contact to WWAN

contact to WLAN

contact to Express card

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SATA_RN0/PERN6_L3
SATA_RP0/PERP6_L3
SATA_TN0/PETN6_L3
SATA_TP0/PETP6_L3
SATA_RN1/PERN6_L2
SATA_RP1/PERP6_L2
SATA_TN1/PETN6_L2
SATA_TP1/PETP6_L2
SATA_RN2/PERN6_L1
SATA_RP2/PERP6_L1
SATA_TN2/PETN6_L1
SATA_TP2/PETP6_L1
SATA_RN3/PERN6_L0
SATA_RP3/PERP6_L0
SATA_TN3/PETN6_L0
SATA_TP3/PETP6_L0

PCIE_PRX_WIGIGTX_N8_L0
PCIE_PRX_WIGIGTX_P6_L0
PCIE_PTX_WIGIGRX_N8_L0
PCIE_PTX_WIGIGRX_P6_L0

SATA0GP/GPIO34
SATA1GP/GPIO35
SATA2GP/GPIO36
SATA3GP/GPIO37
SATA_IREF
RSVD
SATA_RCOMP
SATALED

SATA_ACT#
LANCLK_REQ#

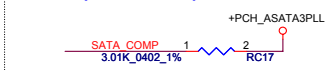
MCARD_PCIE#_SATA_R6
MPCIE_RST#
HDD_DET#

PCIE_RST#
HDD_DET#

PCIE_RST#
HDD_DET#

PCIE_RST#
HDD_DET#

SATA Impedance Compensation



CAD note:

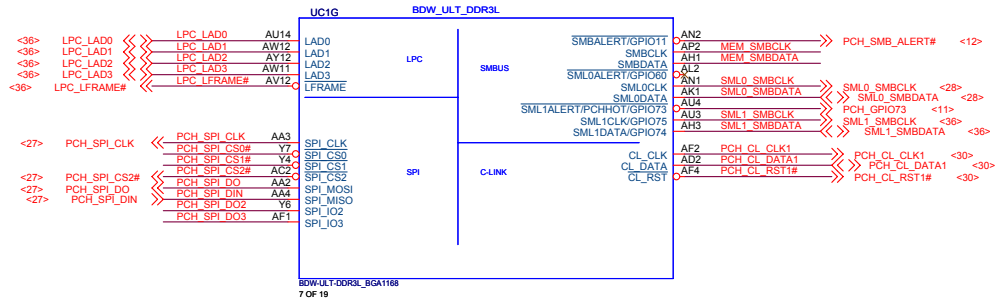
Place the resistor within 500 mils of the PCH. Avoid routing next to clock pins.

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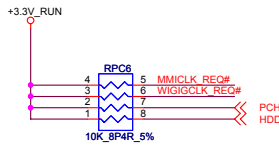
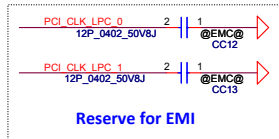
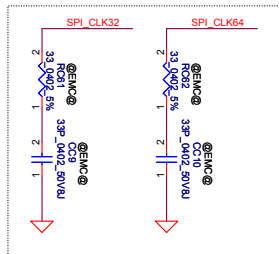


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SOFTWARE TAA



PCIECLK for DSC

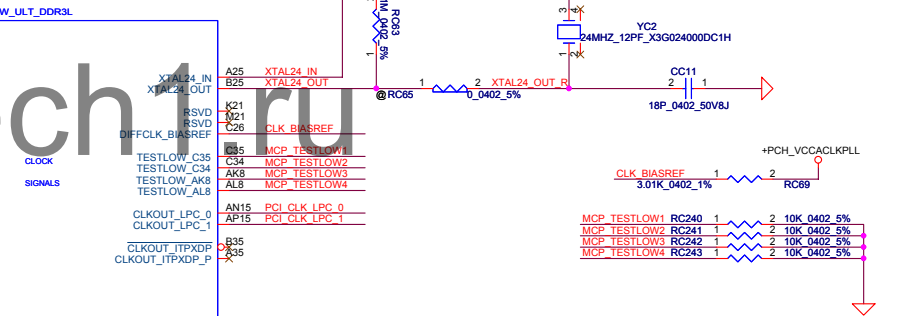
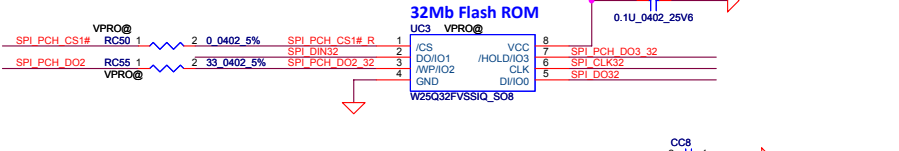
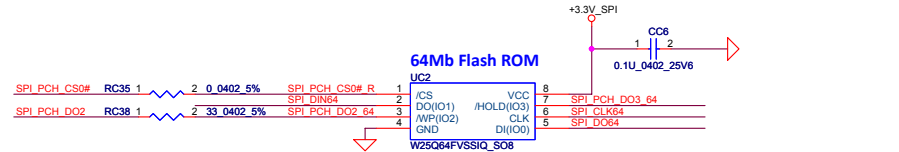
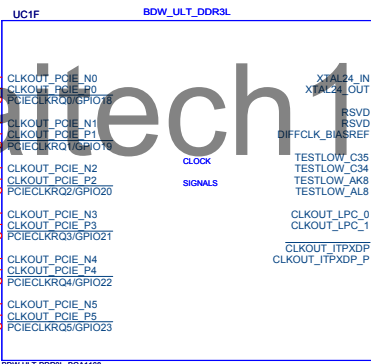
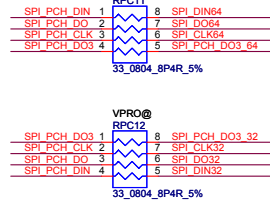
MMI ---->

10/100/1G LAN ---->

WLAN (NGFF1) ---->

GPU ---->

WIGIG (NGFF1) ---->

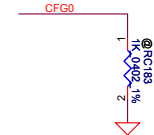
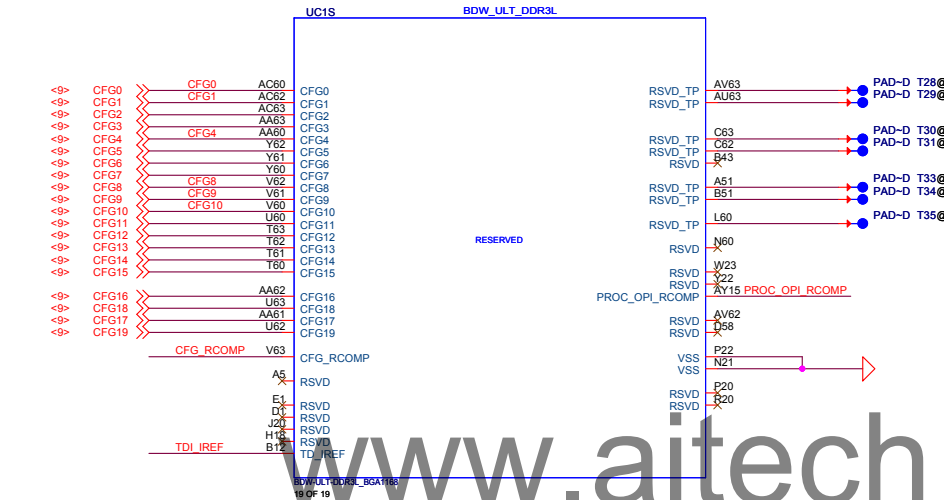


support SPI TPM	
LPC_0	LPC_1
SIO	DOCK
MEC	DEBUG

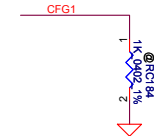
PCB	PCIE1	PCIE2	PCIE3	PCIE4	PCIE5	PCIE6
H12 UMA	SD card	NA	LOM	WIGIG	WIGIG	M2 3042 (HCA & SATA-Cache)
H12 Entry	SD card	NA	LOM	WLAN	WIGIG	NA
H14 DSC	SD card	NA	LOM	WLAN	GPU	WIGIG
H14 UMA	SD card	NA	LOM	WLAN	WIGIG	M2 3042 (HCA & SATA-Cache)
H14D_En	SD card	NA	LOM	WLAN	GPU	WIGIG
H14U_En	SD card	NA	LOM	WLAN	WIGIG	NA
H15 DSC	SD card	NA	LOM	WLAN	GPU	WIGIG
H15 UMA	SD card	NA	LOM	WLAN	WIGIG	M2 3042 (HCA & SATA-Cache)
H15D_En	SD card	NA	LOM	WLAN	GPU	WIGIG
H15U_En	SD card	NA	LOM	WLAN	WIGIG	Express card

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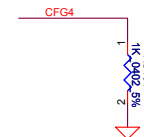
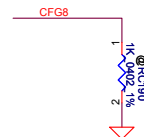
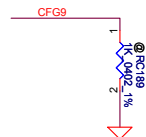
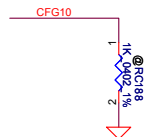
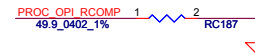
CFG STRAPS for CPU



EAR-STALL/NOT STALL RESET SEQUENCE AFTER PCU PLL IS LOCKE	
CFG0	1:(Default) Normal Operation; No stall 0:Lane Reversed



PCH/PCH LESS MODE SELECTION	
CFG1	1:(Default) Normal Operation 0:Lane Reversed



SAFE MODE BOOT	
CFG10	<p>1: POWER FEATURES ACTIVATED DURING RESET</p> <p>0: POWER FEATURES (ESPECIALLY CLOCK GATINE ARE NOT ACTIVATED</p>

NO SVID PROTOCOL CAPABLE VR CONNECTED	
CFG9	<p>1: VRs support SVID protocol are present</p> <p>0: No VR support SVID is present</p> <p>The chip will not generate (OR Respond to) SVID activity</p>

ALLOW THE USE OF NOA ON LOCKED UNITS	
CFG8	1: Enable(Default): Noa will be disable in locked units and enable in un-locked units. 0: Disable Noa will be available regardless of the locking of the unit

	Display Port Presence Strap
CFG4	1 : Disabled; No Physical Display Port attached to Embedded Display Port
	0 : Enabled; An external Display Port device is connected to the Embedded Display Port

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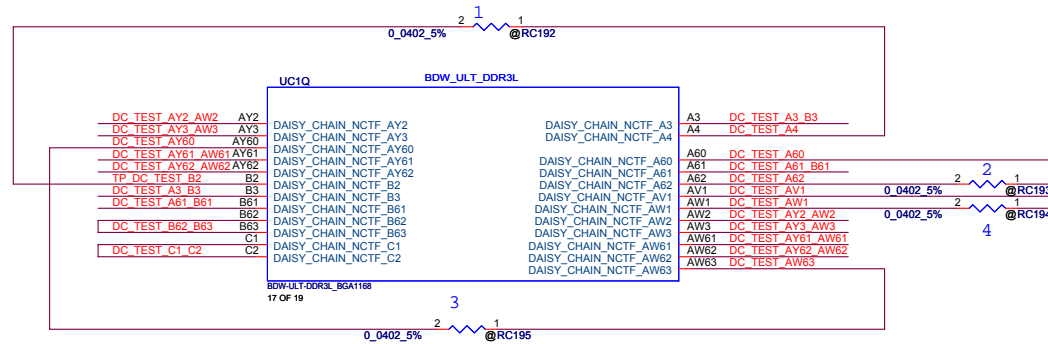


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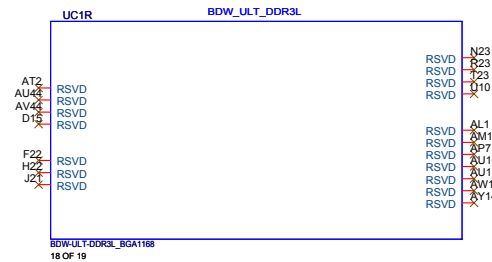
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Package Daisy Chain:

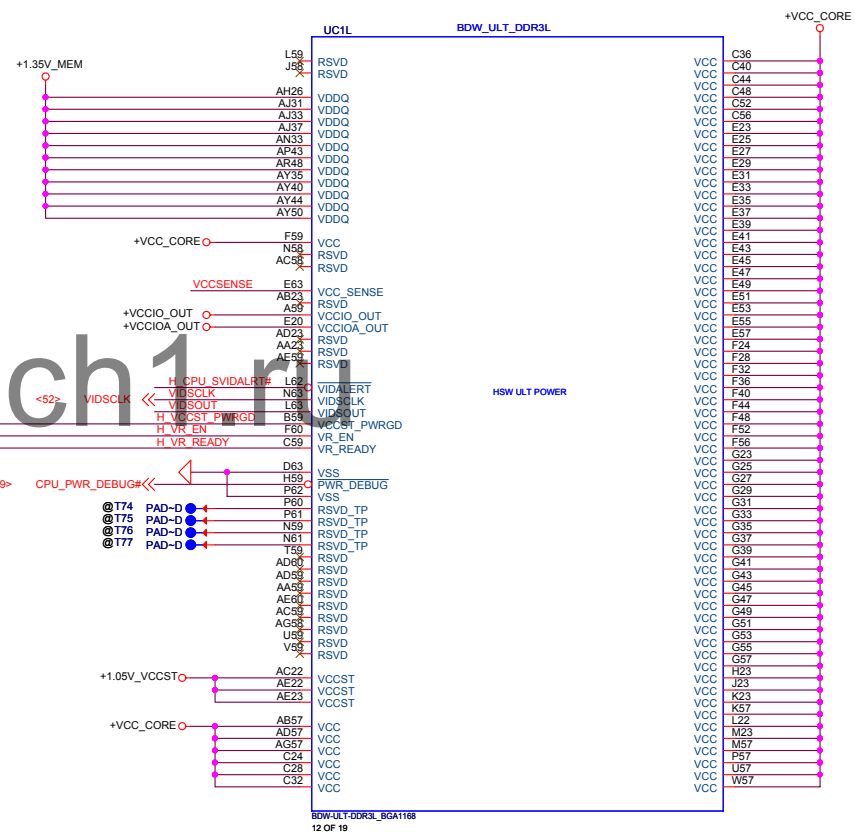
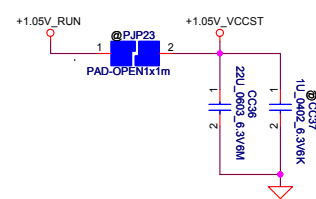
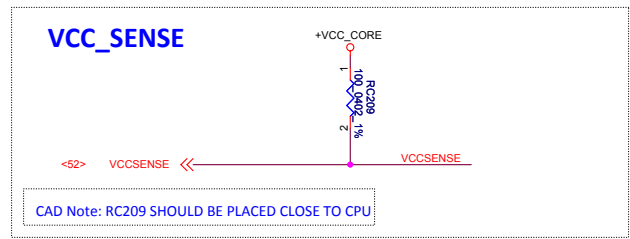
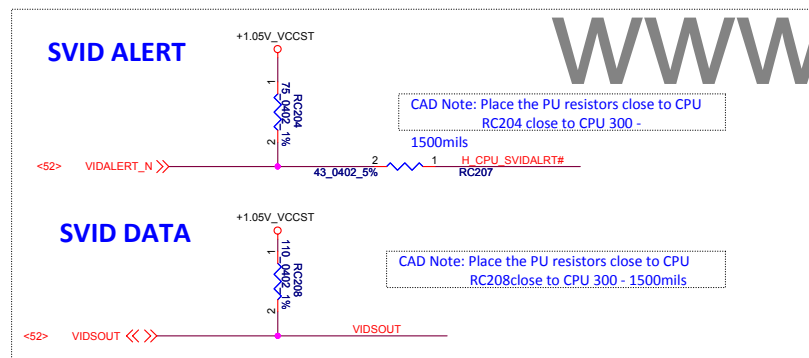
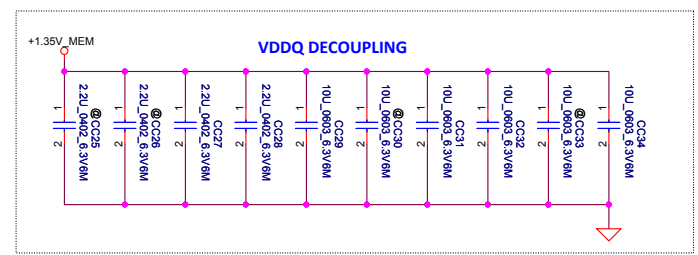
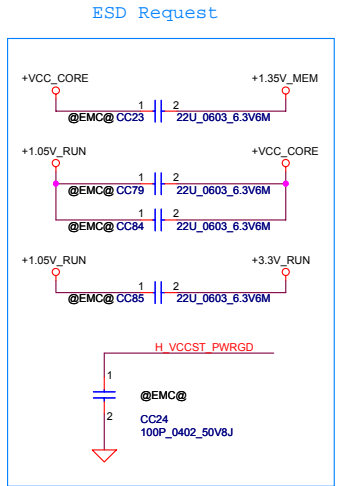
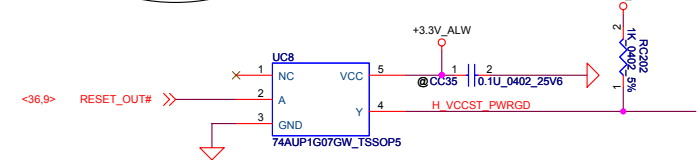
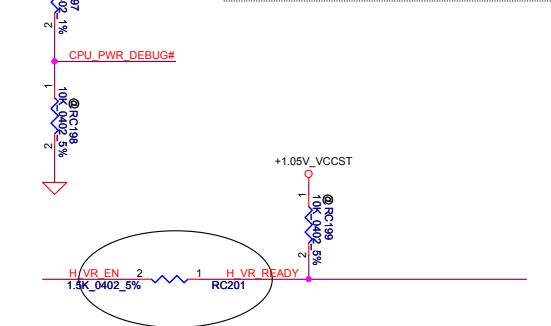
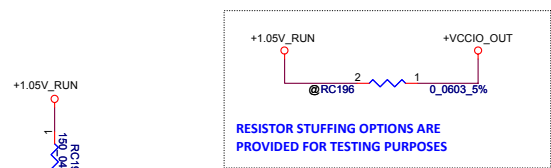
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- 3.AY60-PKG-AW61-PCB-AY61-PKG-AW62-PCB-AY62-PKG-AW63
- 4.AW1-PKG-AW3-PCB-AY3-PKG-AW2-PCB-AY2-PKG-AV1

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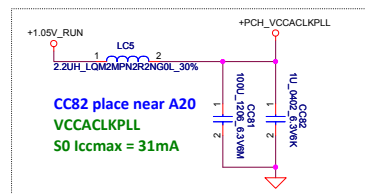
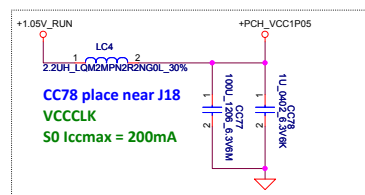
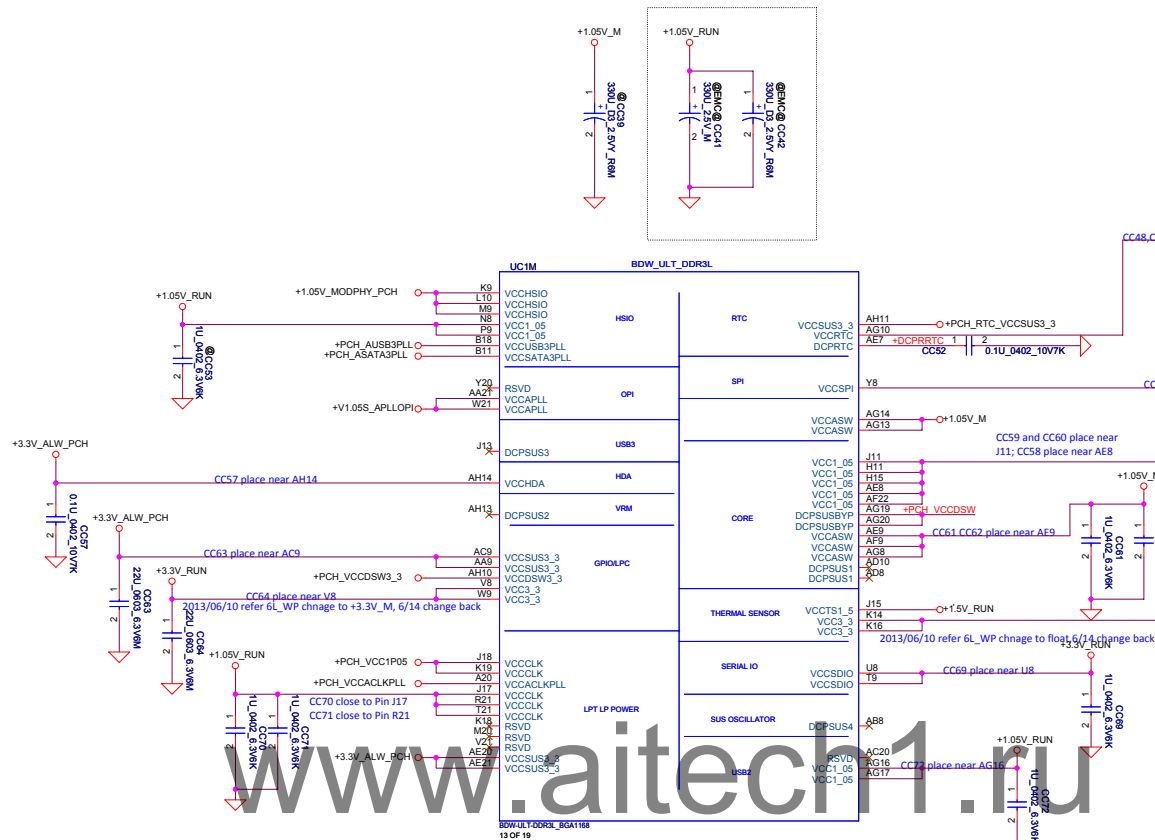
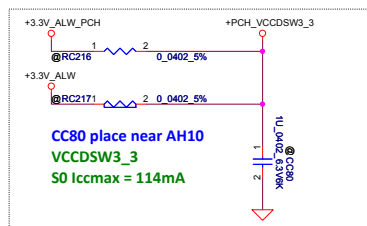
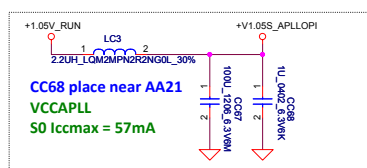
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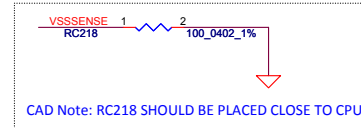
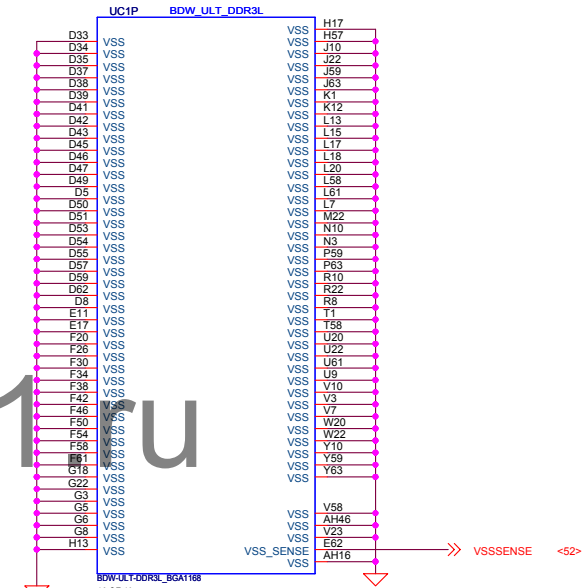
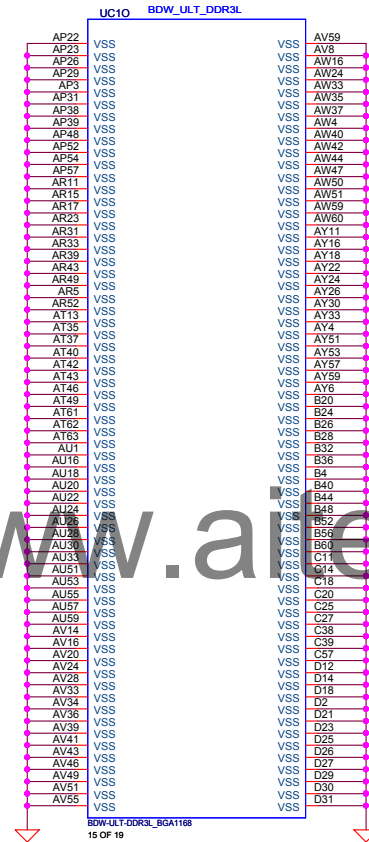
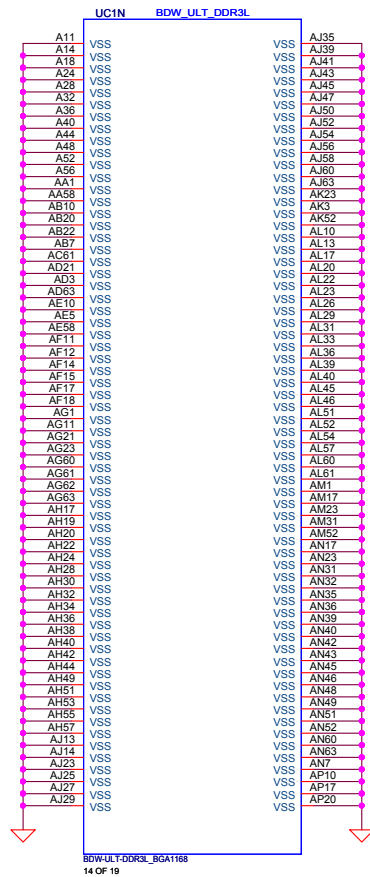
Voltage Rail	Voltage (V)	30 Iccmax Current (A) ³	5x Iccmax Current (A) ³	Deep 5x Iccmax (A) ³	G3
VCC1_05 (Internal Suspend VR mode using INTVRMEN)	1.05	1.741	0	0	0
VCC1_05 (External Suspend VR mode using INTVRMEN)	1.05	1.632	0	0	
VCCAPLL	1.05	0.057	0	0	0
VCCSATA3PLL	1.05	0.042	0	0	0
VCCUSB3PLL	1.05	0.041	0	0	0
VCCCLKPLL	1.05	0.031	0	0	0
VCCCLK	1.05	0.200	0	0	0
VCCHSIO	1.05	1.838	0	0	0
VCCTS1_5	1.5	0.003	0	0	0
VCC3_3	3.3	0.041	0	0	0
VCCSDIO	3.3	0.017	0	0	0
VCCAEW	1.05	0.458	0	0	0
VCCSPI	3.3	0.018	0	0	0
VCCIDA	3.3	0.011	<1 mA	0	0
VCCSUS3_3 (Internal Suspend VR mode using INTVRMEN)	3.3	0.063	0.024	0	0
VCCSUS3_3 (External Suspend VR mode using INTVRMEN)	3.3	0.062	0.009	0	0
DcpSus1 ⁴	1.05	0.109	0.014	0	0
DcpSus2 ⁴	1.05	0.025	0.001	0	0
DcpSus3 ⁴	1.05	0.010	0.003	0	0
DcpSus4 ⁴	1.05	0.001	0.001	0	0
VCCDSW3_3	3.3	0.114	0.004	0.002	0
VCCRTC	3.3	<1 mA	<1 mA	<1 mA	6 μ A See note 1, 2

Voltage Supply	Interface (power rail isolation required)	PCB Pin sharing power rail
V1.05s	Case OPT K9, L10, M0, P0, S10, S11, M9 U000 AG05, AG07 CLAPL A20 CLK(A) CLK(B) CLK(C)	J11, H11, H15, A08, A72 AA21, W21 K9, L10, M0, P0, S10, S11, M9 AG05, AG07 A20 R21, T21 J08, K19 J17
V3.3s	GPIO BTC H0A AP04	AC9, AA9, AE20, AE21 AP01 AP04
V3.3s	GPIO SD00 Thermal Sensor	W8, W9 U8, T9 K14, K16

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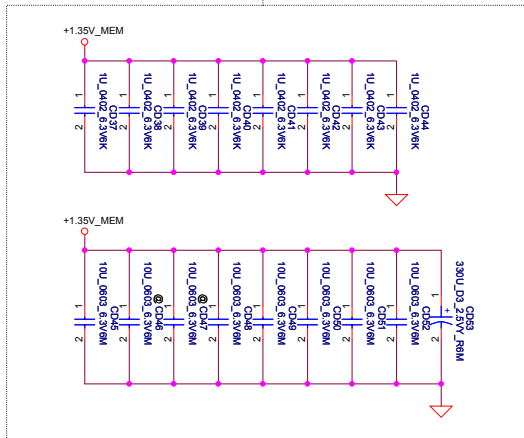
Size: **4019RB**

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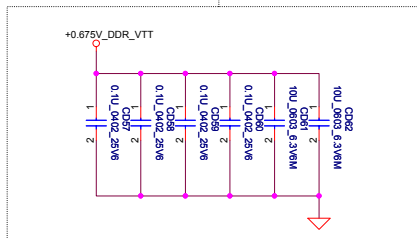


 DDR_B_DQS#0..7 <<>>
 DDR_B_DQ0..63 <<>>
 DDR_B_DQS#0..7 <<>>
 DDR_B_MA0..15 <<>>

Layout Note:
Place near JDIMM2



Layout Note:
Place near
JDIMM2.203,204



Note:
Check voltage tolerance of
VREF_DQ at the DIMM socket

+3.3V_RUN

+0.675V_DDR_VTT

+3.3V_RUN

+0.675V_DDR_VTT

+0.675V_DDR_VTT

+0.675V_DDR_VTT

+0.675V_DDR_VTT

+0.675V_DDR_VTT

+0.675V_DDR_VTT

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+0.675V_DDR_VTT

+0.675V_DDR_VTT

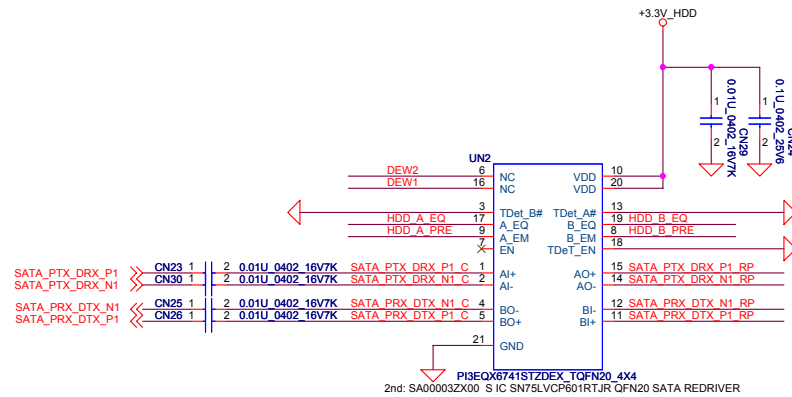
+0.675V_DDR_VTT

SP07000P700 LI NK DONE

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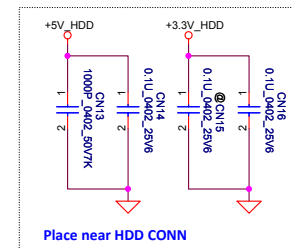
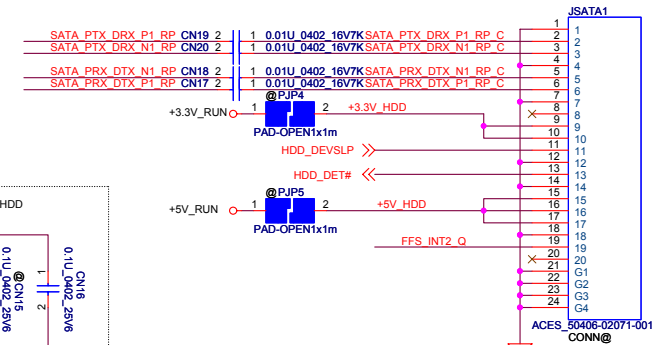
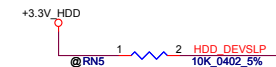
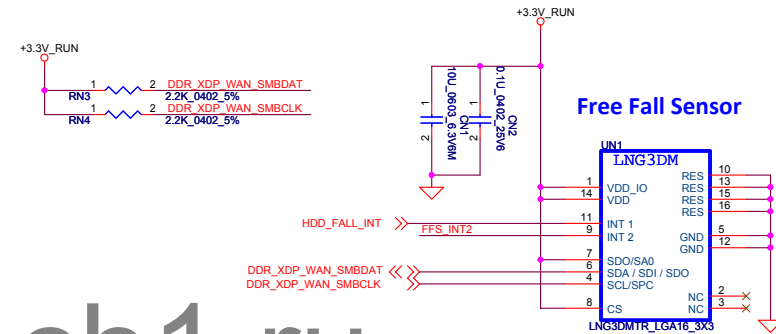
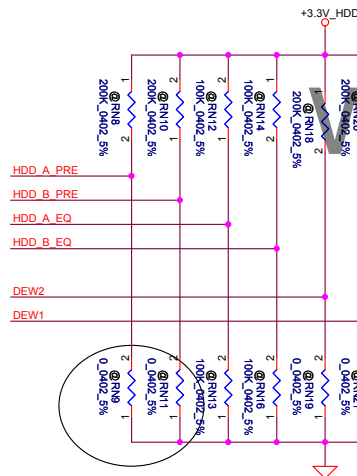
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SATA Repeater



PERICOM PI3EQX6741ST:
Pin6/16, NC
Pin8/9, Pre-emphasis

TI SN75LVCP601RTJR
Pin6/16, de-emphasis width setup
Pin8/9, de-emphasis



SP010016L00 LI NK DONE

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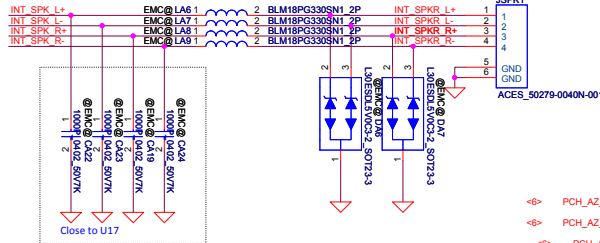
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SP02000W/00 LINK DONE

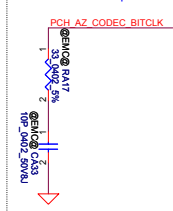
1W x 1ch, 4ohm (Transducer spec is 8Ohm/0.5Watt per unit, there are two transducer units in one speaker box.)

Internal Speakers Header

40 mils trace keep 20 mil spacing



Close to U17 pin6

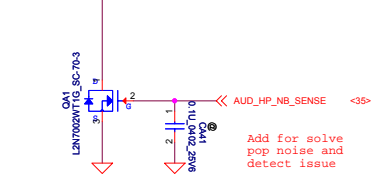


BCLK: Audio serial data bus bit clock input/output
LRCK: Audio serial data bus word clock input/output

<35> AUD_NB_MUTE# >>_____

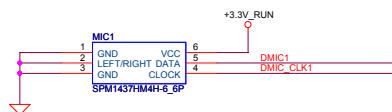
Place closely to Pin 13.

AUD_SENSE_A

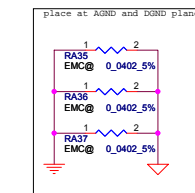


Add for solve
pop noise and
detect issue

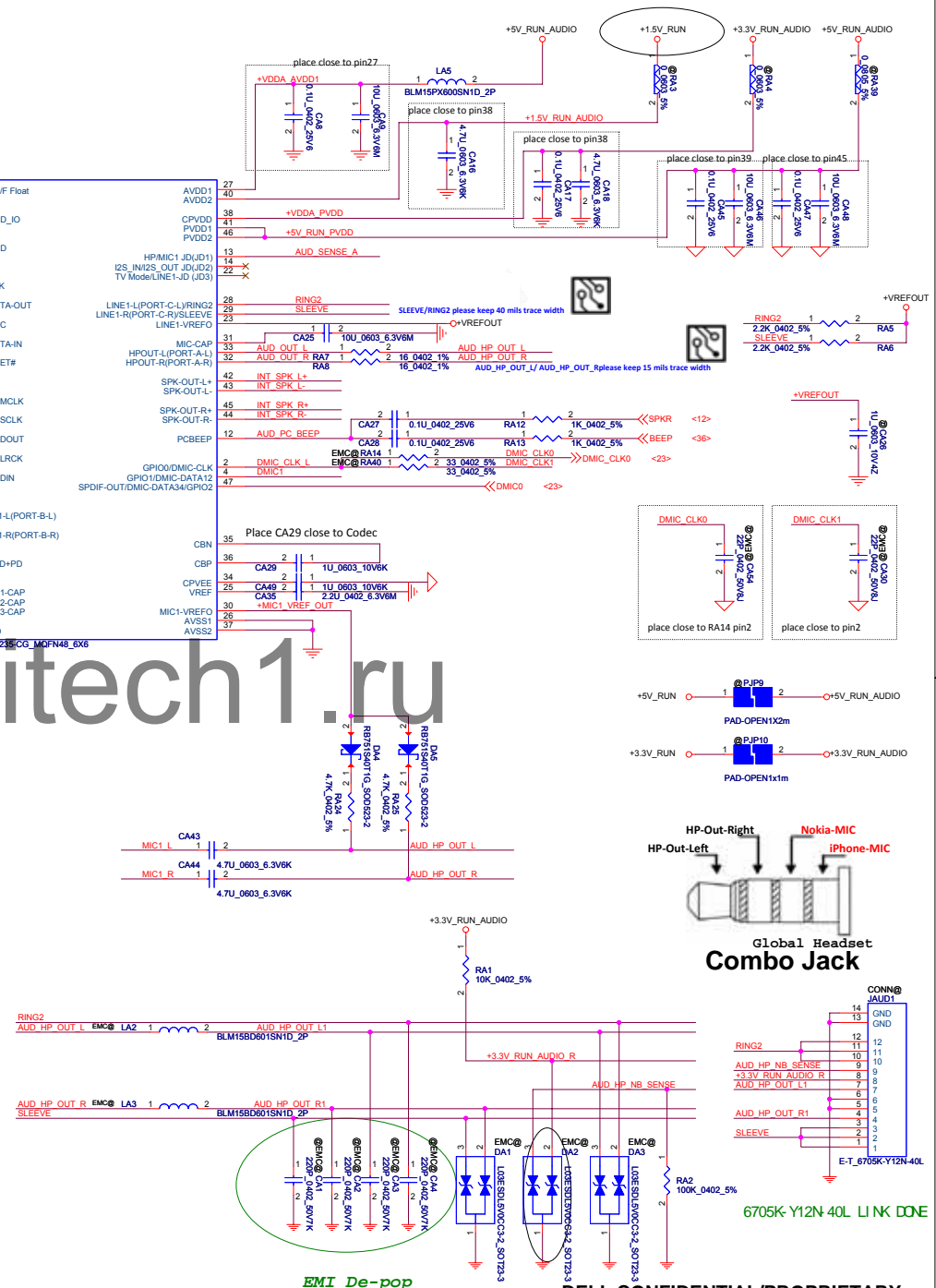
Digital Mic



Realtek feedback
Prevent the Noise from Combo Jack
while system entry into S3 / S4 / S5



A schematic diagram of a component labeled "PNP6". It consists of two blue rectangular blocks connected by a horizontal line. The left block is labeled "1" and the right block is labeled "2". Below the blocks is the text "PAD-OPEN1x2m". The component is connected to a ground symbol on the left and a voltage source symbol on the right.



Global Headset
Combo Jack

CONN@ JAUD1

Pin	Signal
14	GND
13	GND
12	RING2
11	AHD_HP_NB_SENSE
10	+3.3V RUN AUDIO R
9	AHD_HP_OUT_L1
8	AHD_HP_OUT_R1
7	SLEEVE
6	GND
5	GND
4	GND
3	GND
2	GND
1	GND

E-T 6705K-Y12N-40L

6705K- Y12N 40L LI NK DONE

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4019BB

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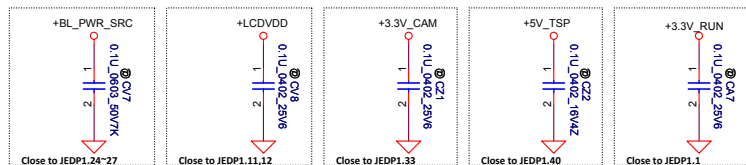
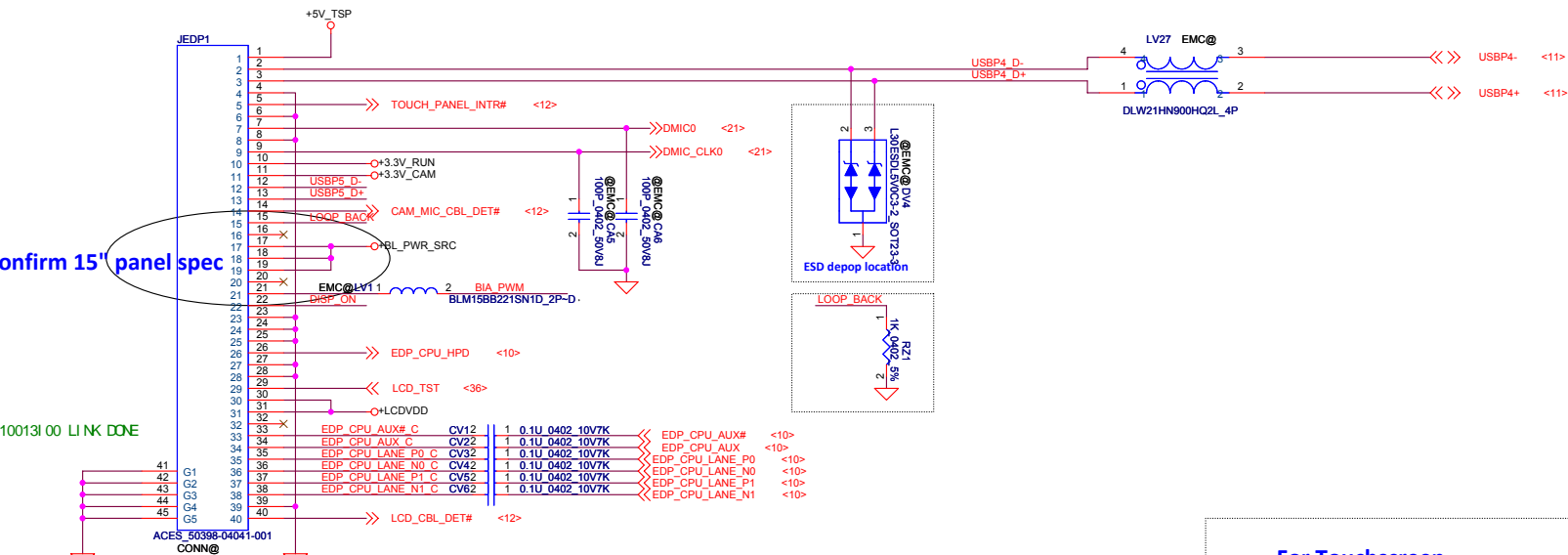


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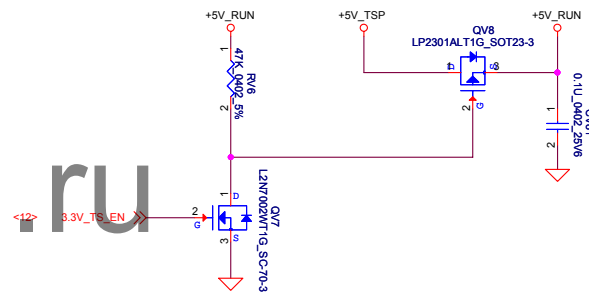
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confirm 15" panel spec

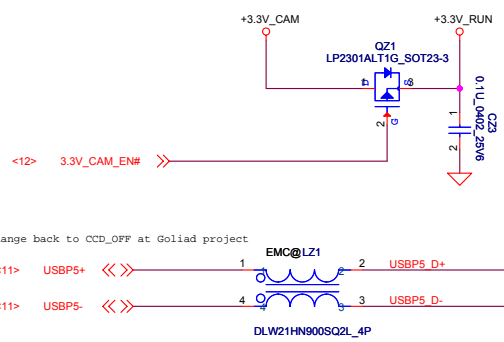
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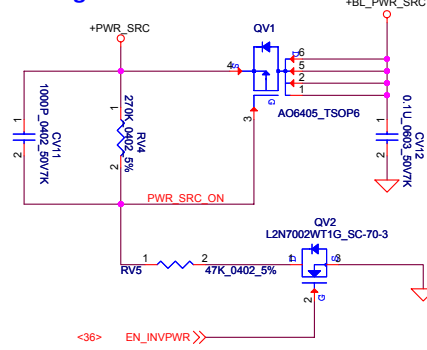
For Touchscreen



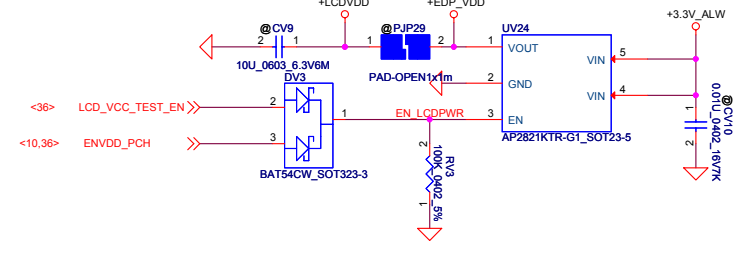
WebCAM



Backlight POWER



LCDVDD POWER



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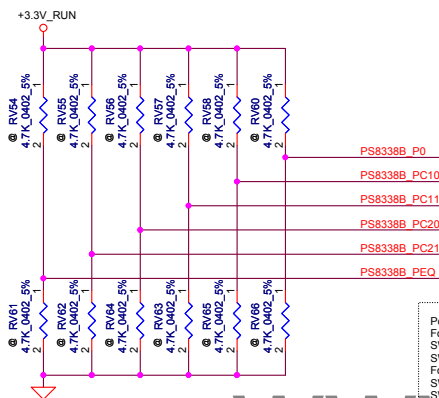
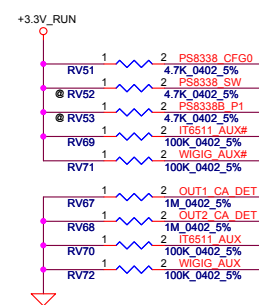
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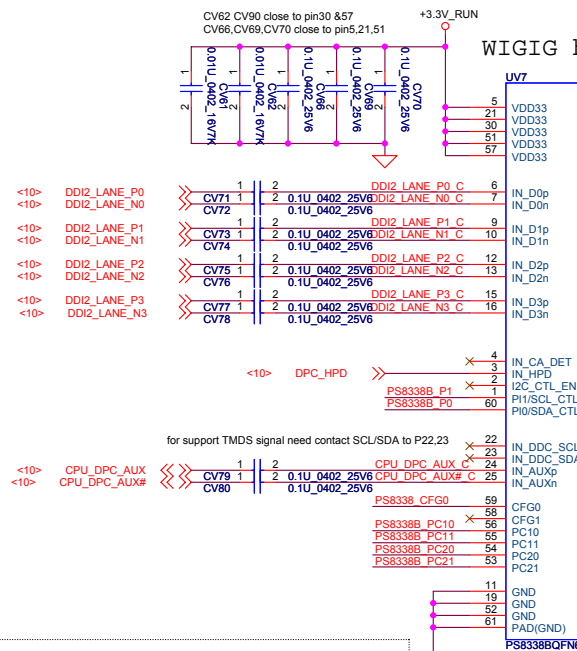
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14"/15" use 12412 at Entry config

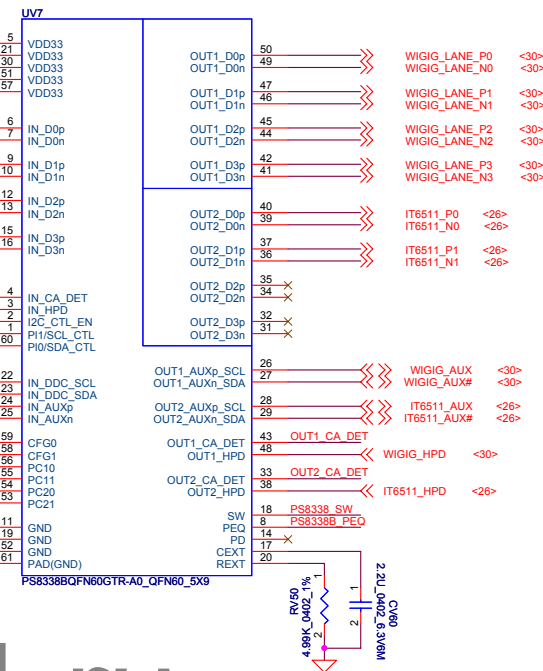
PCB	DP SWITCH
H12 UMA	PS8339+DP12412
H12 Entry	PS8339
H14 DSC	PS8338
H14 UMA	PS8338
H14D_En	DP12412
H14U_En	DP12412
H15 DSC	PS8338
H15 UMA	PS8338
H15D_En	DP12412
H15U_En	DP12412



Port switching control or priority configuration. Internal pull down ~150KΩ, 3.3V I/O
For Control Switching Mode (CFG0 = L):
SW = L: Port1 is selected (default)
SW = H: Port2 is selected
For Automatic Switching Mode (CFG0 = H):
SW = L: Port1 has higher priority when both ports are plugged (default)
SW = H: Port2 has higher priority when both ports are plugged



WIGIG has high priority when both ports plugged



For Automatic Switching Mode (CFG0 = H):
SW = L: Port1 has higher priority when both ports are plugged (default)
SW = H: Port2 has higher priority when both ports are plugged

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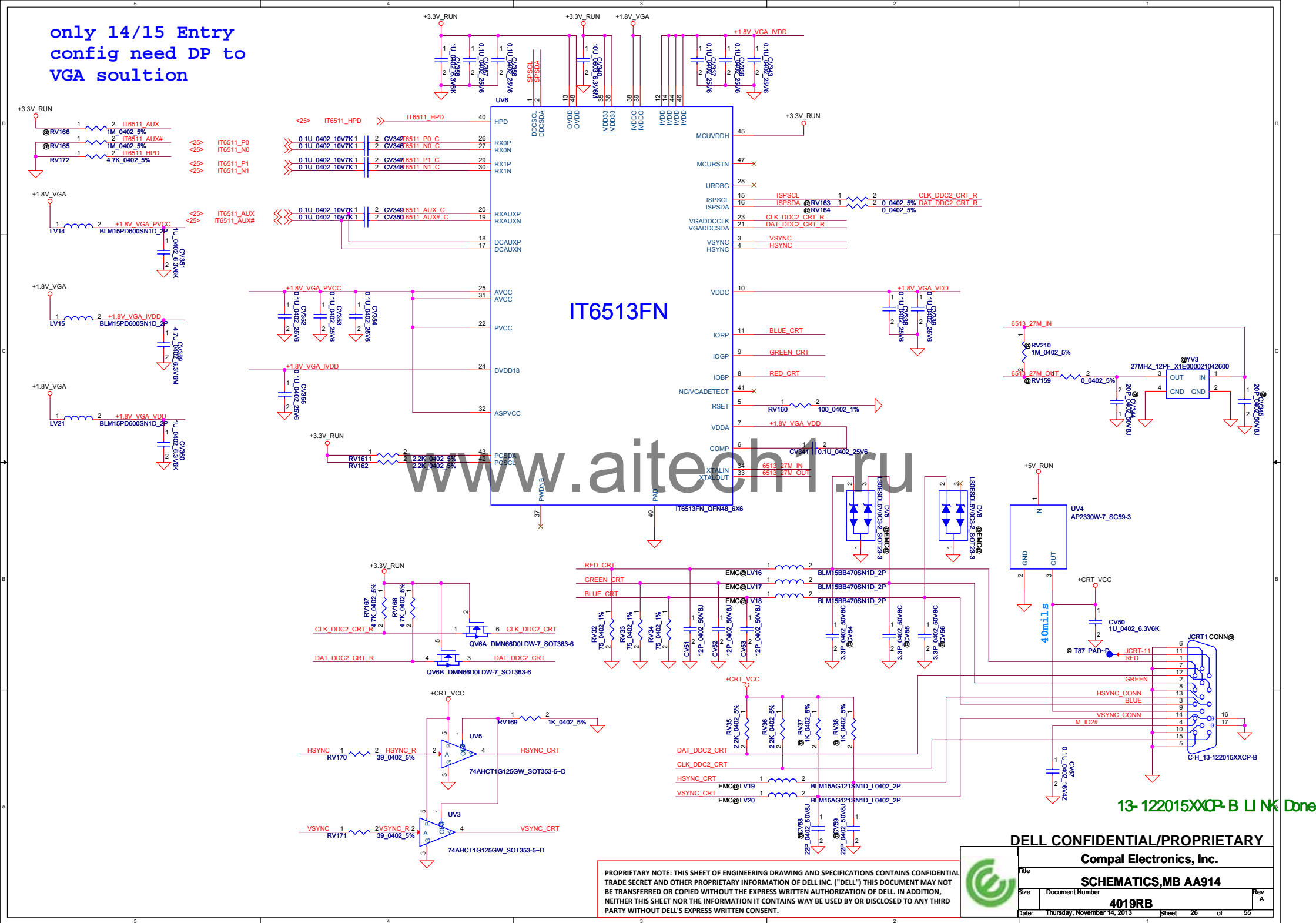
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only 14/15 Entry
config need DP to
VGA solution



13- 122015XXCP- B L I N K Done

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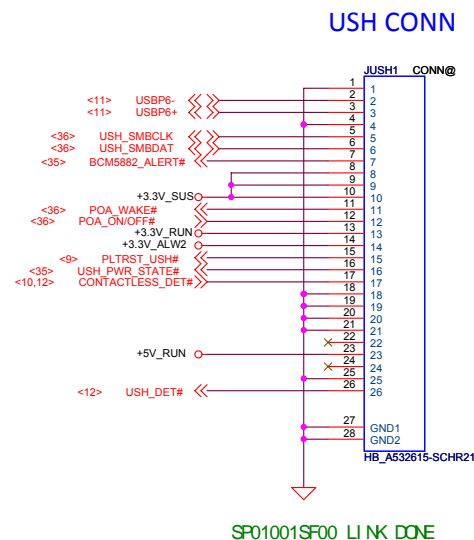
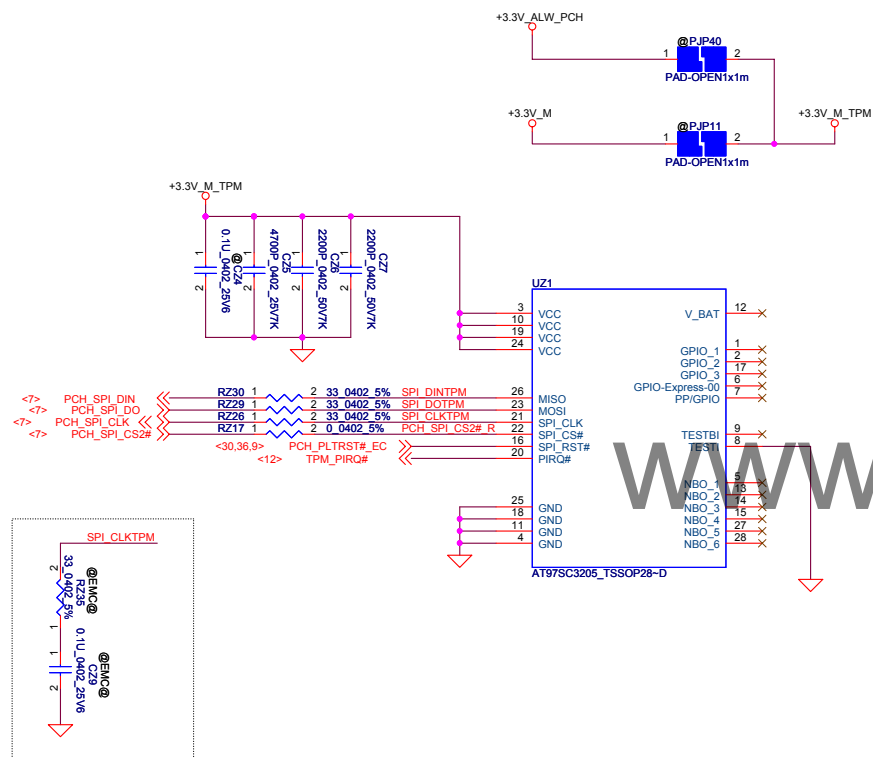
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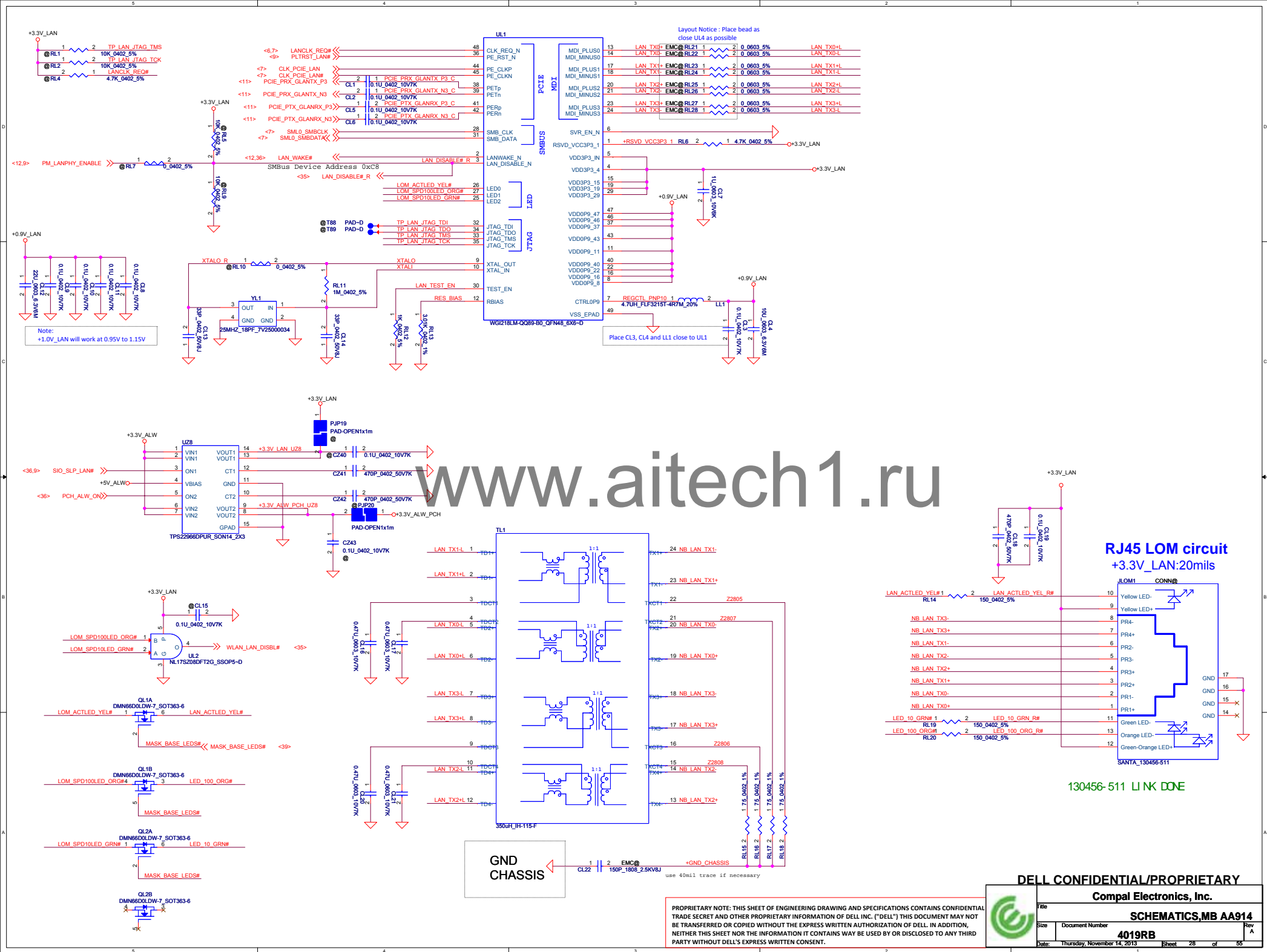


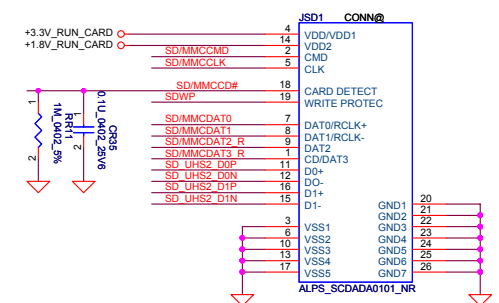
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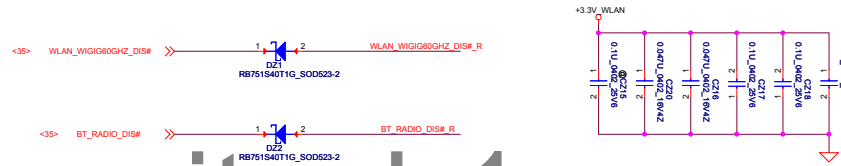
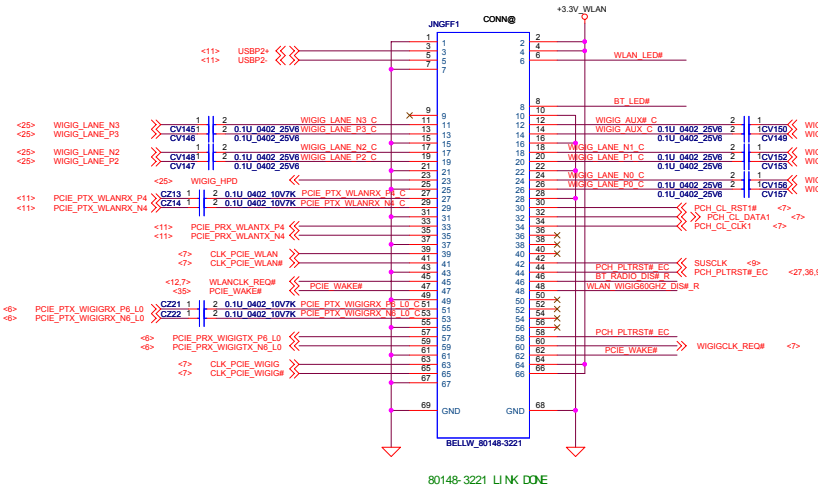


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NGFF for DSC

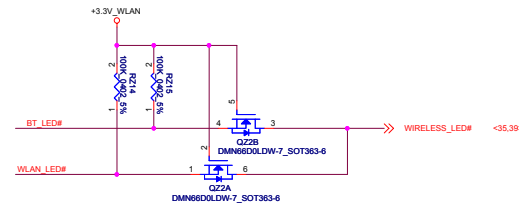
NGFF slot A Key A



Power Rating TBD

PWR Rail	Voltage Tolerance	Primary Power		Aux Power
		Peak	Normal	Normal
+3.3V				

LED control circuit

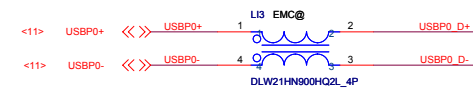
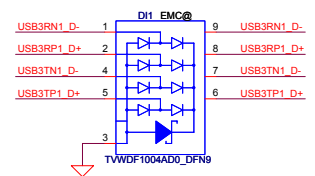
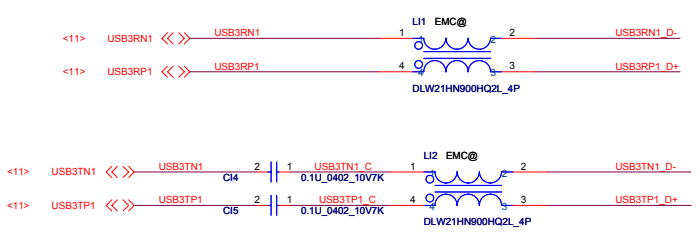


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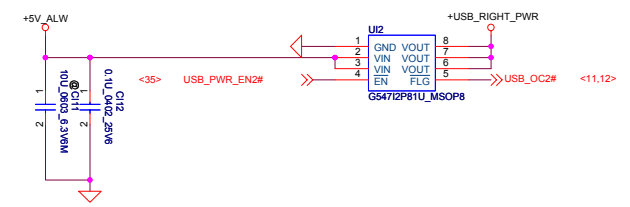
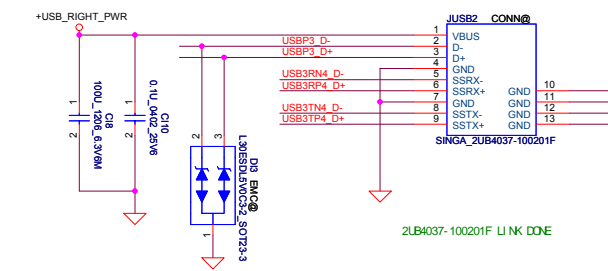
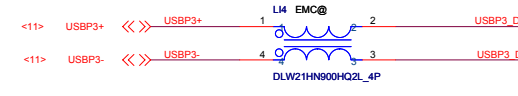
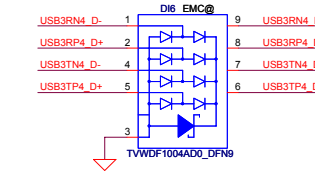
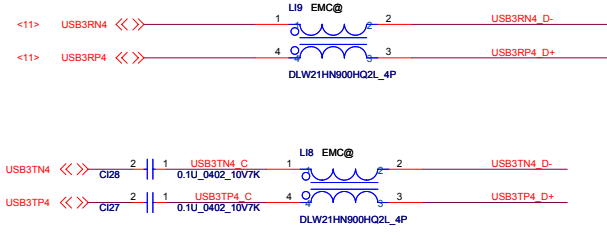
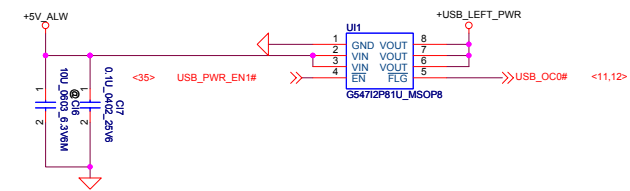
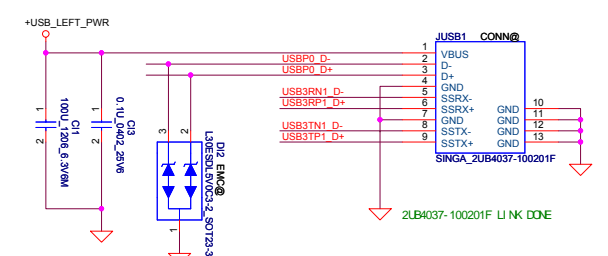
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Size	Document Number	4019RB	
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PCB	USB2 0	USB2 3
H12 UMA	USB3102	NX3DV221
H12 Entry	NA	NA
H14 DSC	USB3102	NX3DV221
H14 UMA	USB3102	NX3DV221
H14D_En	NA	NA
H14U_En	NA	NA
H15 DSC	USB3102	NX3DV221
H15 UMA	USB3102	NX3DV221
H15D_En	NA	NA
H15U_En	NA	NA



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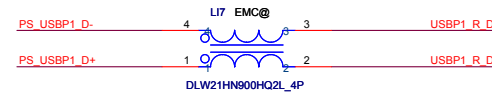
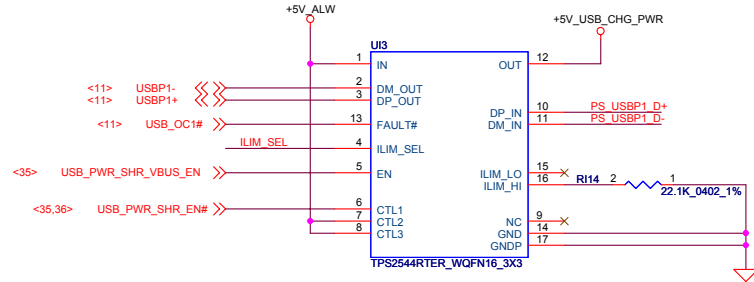
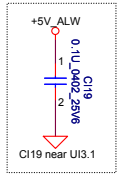
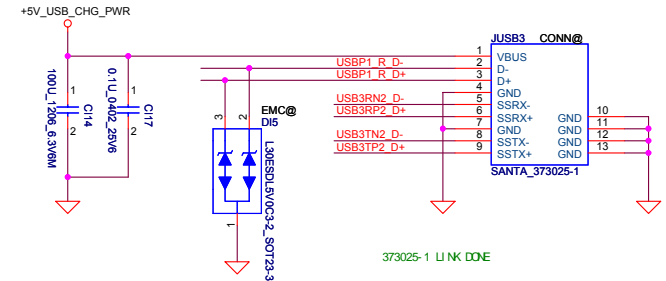
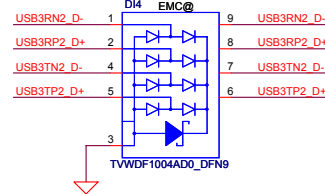
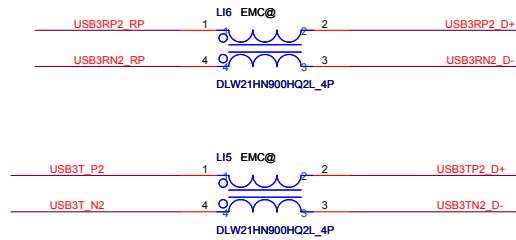
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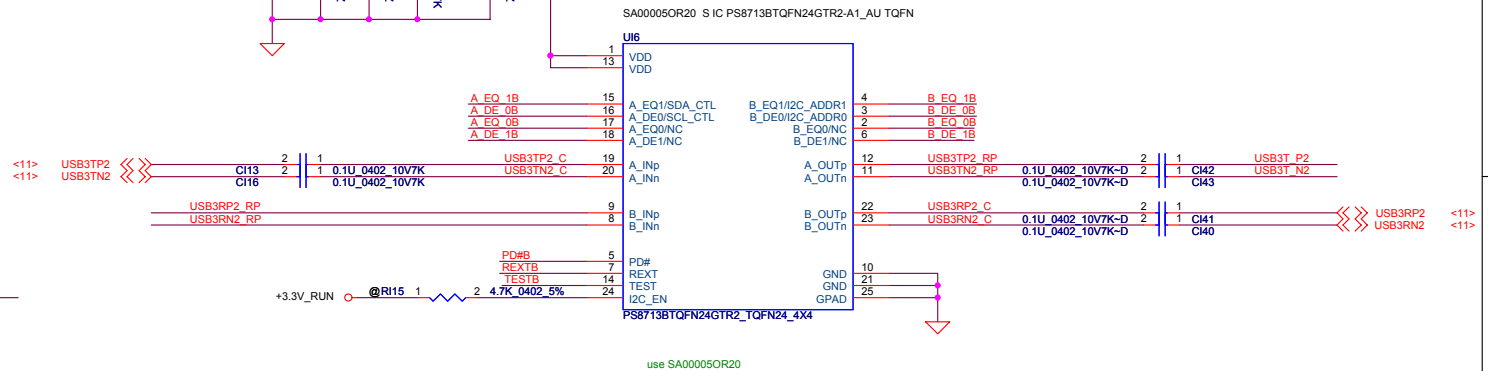
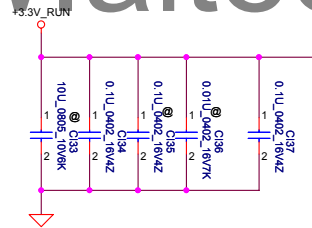
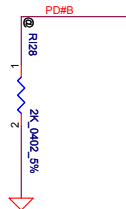
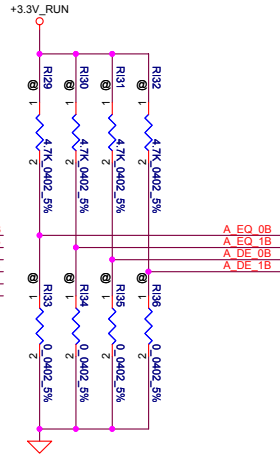
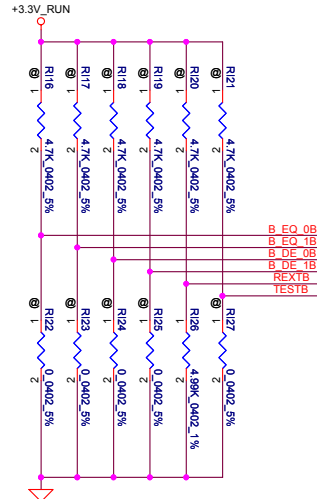


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 USB3 Repeater



Doesn't support.

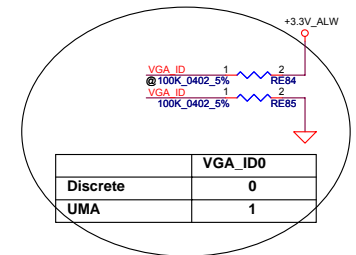
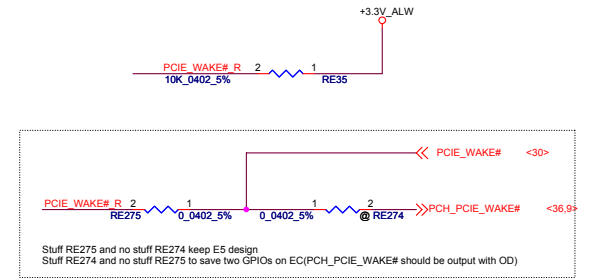
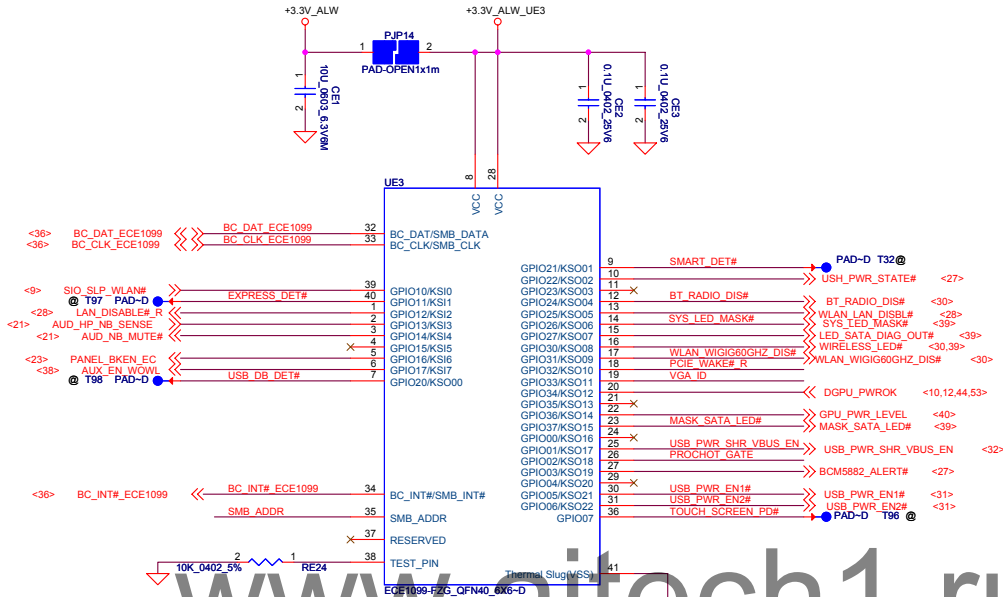
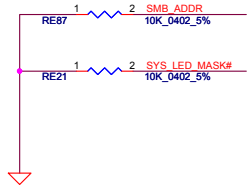
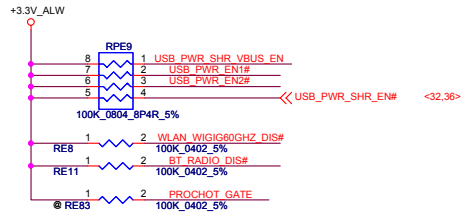
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	VGA_ID0
Discrete	0
UMA	1

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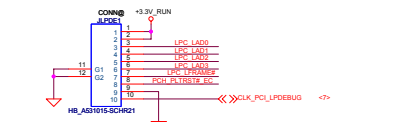
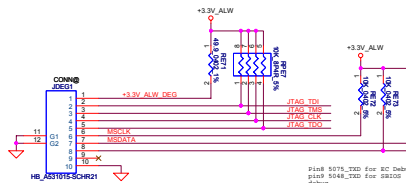
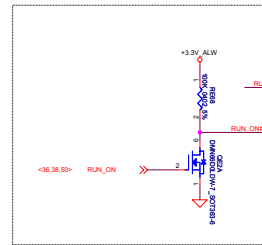
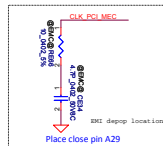
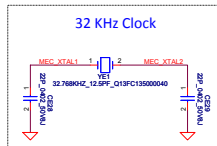
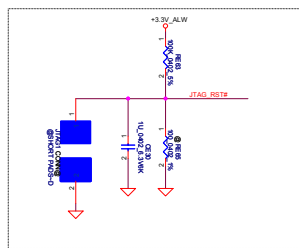
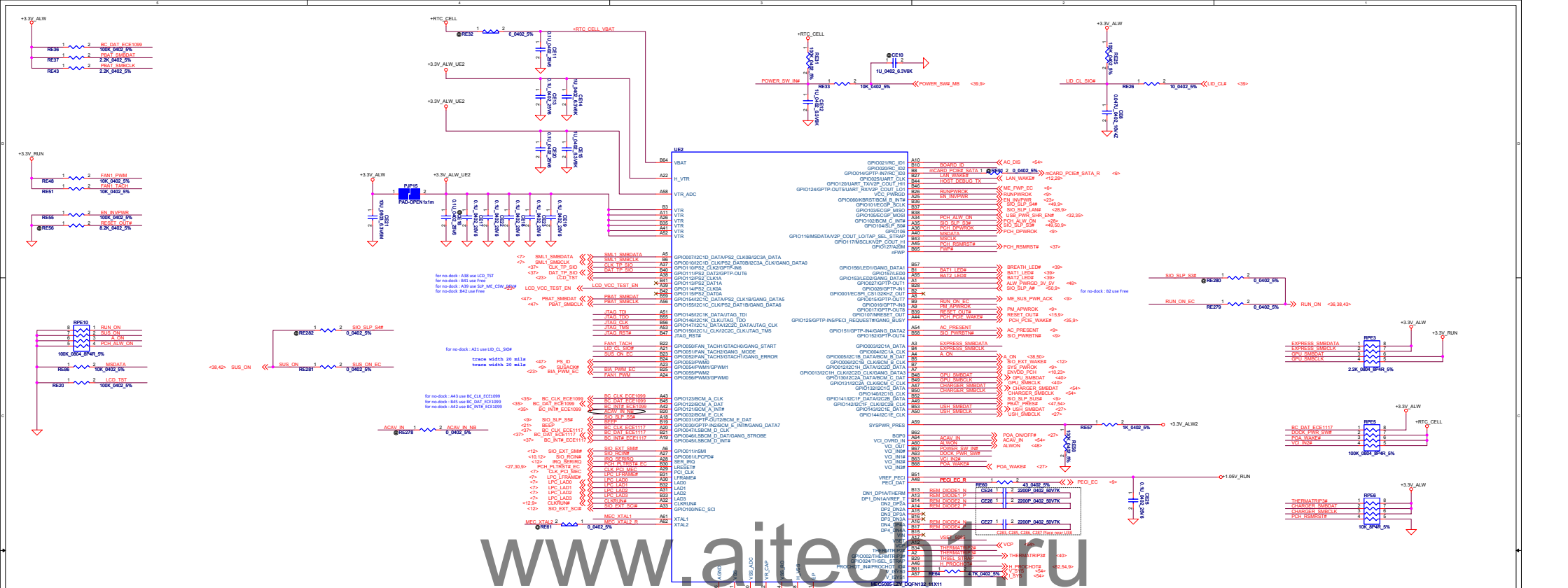
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REV	CE40	REV
240K	4700p	X00
130K	4700p	X01
33K	4700p	X02
1K	4700p	A00

BOARD ID rise time is measured from 5%-68%

Setting for Thermal Design

5085 Channel	Location
DP1/DN1	CPU
DP2/DN2	DIMM
DN2a/DP2a	WIGIG
DP4/DN4	V.R

Place under CPU
Place CE35 close to the QE3 as possible

DP2/DN2 for SODIMM on QE5, place QE5 close to SODIMM and CE37 close to QE5

DN2a/DP2a for WIGig on QE7, place QE7 close to WIGig and CE46 close to QE7

DP4/DN4 for Skin on QE6, place QE6 close to Vcore VR choke.

Place CE35 close to the QE3 as possible

DP2/DN2 for SODIMM on QE5, place QE5 close to SODIMM and CE37 close to QE5

DN2a/DP2a for WIGig on QE7, place QE7 close to WIGig and CE46 close to QE7

DP4/DN4 for Skin on QE6, place QE6 close to Vcore VR choke.

Place CE35 close to the QE3 as possible

DP2/DN2 for SODIMM on QE5, place QE5 close to SODIMM and CE37 close to QE5

DN2a/DP2a for WIGig on QE7, place QE7 close to WIGig and CE46 close to QE7

DP4/DN4 for Skin on QE6, place QE6 close to Vcore VR choke.

Place CE35 close to the QE3 as possible

DP2/DN2 for SODIMM on QE5, place QE5 close to SODIMM and CE37 close to QE5

DN2a/DP2a for WIGig on QE7, place QE7 close to WIGig and CE46 close to QE7

DP4/DN4 for Skin on QE6, place QE6 close to Vcore VR choke.

Place CE35 close to the QE3 as possible

DP2/DN2 for SODIMM on QE5, place QE5 close to SODIMM and CE37 close to QE5

DN2a/DP2a for WIGig on QE7, place QE7 close to WIGig and CE46 close to QE7

DP4/DN4 for Skin on QE6, place QE6 close to Vcore VR choke.

Place CE35 close to the QE3 as possible

DP2/DN2 for SODIMM on QE5, place QE5 close to SODIMM and CE37 close to QE5

DN2a/DP2a for WIGig on QE7, place QE7 close to WIGig and CE46 close to QE7

DP4/DN4 for Skin on QE6, place QE6 close to Vcore VR choke.

Place CE35 close to the QE3 as possible

SF02000TS00 LI NK DONE

reserve for DC fan

reserve for DC fan

reserve for DC fan

reserve for DC fan

reserve for DC fan

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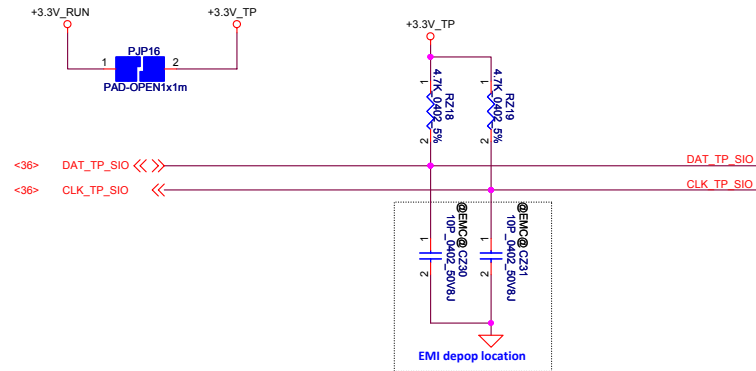
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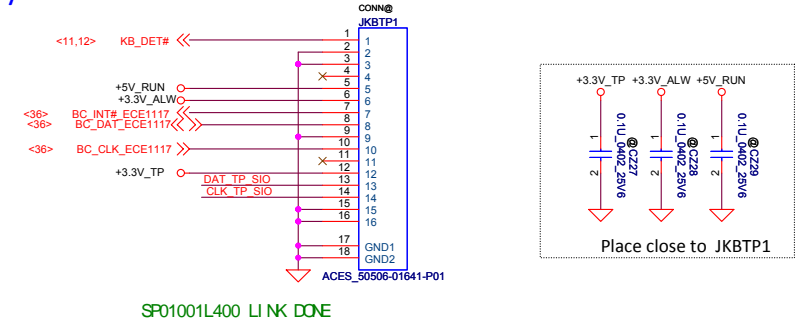
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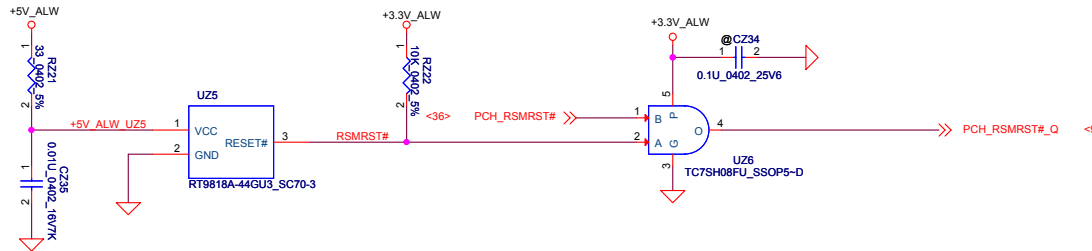
Touch Pad



Keyboard



RSMRST circuit



@eDP Cable

Part Number	Description
DC02C007A00	H-CONN SET 13M MB-EDP

@eDP Cable w camera

Part Number	Description
DC02C007900	H-CONN SET 13M MB-EDP-CAMERA

@eDP TS Cable w camera

Part Number	Description
DC02C007800	H-CONN SET 13M MB-EDP-CAMERA-TS

@SATA Cable-Spindle HDD

Part Number	Description
DC02C007800	H-CONN SET 13M MB-SPINDLE HDD

@SATA Cable-mSATA

Part Number	Description
DC02C007700	H-CONN SET 13M MB-MSATA HDD

@DC-IN Cable

Part Number	Description
DC30100MF00	CONN SET 0VN DCJACK-MB 2DW1003-038110

@RTC BATT

Part Number	Description
DC30100MF00	CONN SET 0VN DCJACK-MB 2DW1003-038110

@FAN

Part Number	Description
DC28A000800	FAN SET DAQ20 DC5V AB7405HB-HB3 ADD

@KBTP FFC

Part Number	Description
NBX0001JH00	FFC 16P G P0.5 PAD=0.3 66.5MM MB-TP 13M

@Audio Board FFC

Part Number	Description
NBX0001JP00	FFC 12P F P.5 PAD=0.35 26.85MM MB-AUDIO/B

@USH Board FFC

Part Number	Description
NBX0001JP00	FFC 26P G P0.5 PAD=0.3 58MM MB-USH/B 13M

@LED Board FFC

Part Number	Description
NBX0001JM00	FFC 10P G P.5 PAD.3 192.5MM MB-LED/B 13M

@PWR Board FFC

Part Number	Description
NBX0001JL00	FFC 6P G P0.5 PAD=0.3 31MM MB-PWR/B 13M

@FP FFC-Validity

Part Number	Description
NBX0001JW00	FFC 8P F P0.5 PAD=0.3 170MM USH/B-FP VALIDITY

@FP FFC-TCS

Part Number	Description
NBX0001JW00	FFC 8P F P0.5 PAD=0.3 164.8MM USH/B-FP-TCS

@Speak

Part Number	Description
PK230003Q0L	SPK PACK 2.5X 2.0W 4 OHM PG

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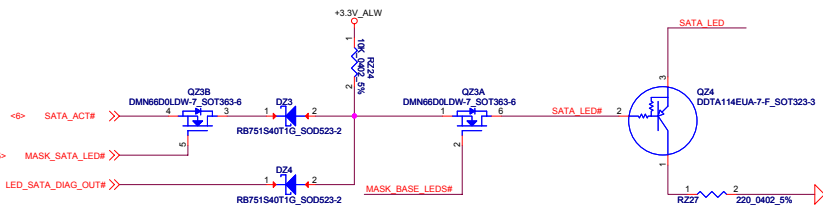


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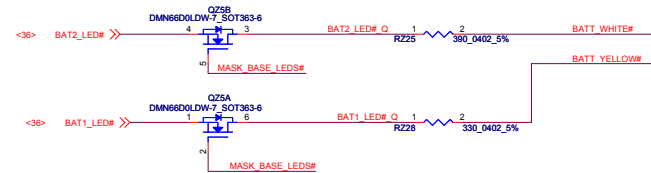
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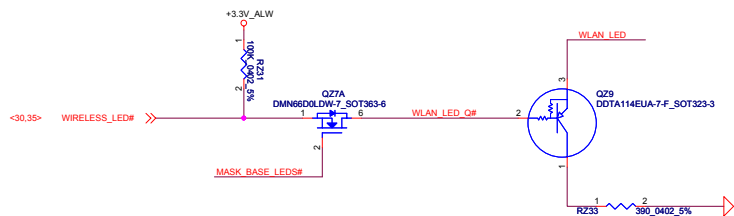
HDD LED solution for White LED



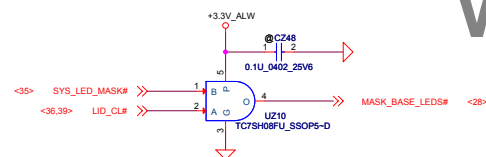
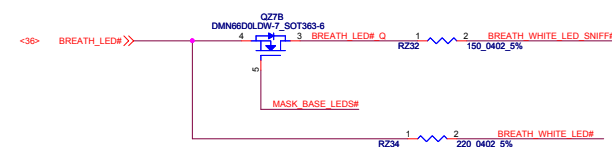
Battery LED



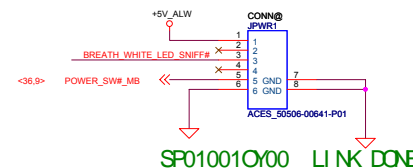
WLAN LED solution for White LED



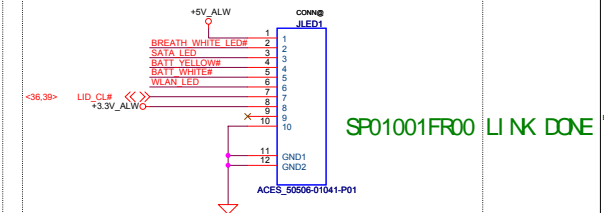
Breath LED



POWER board CONN



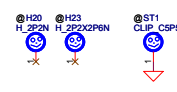
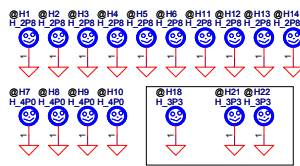
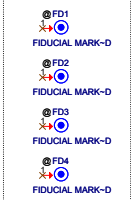
LED board CONN



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LED Circuit Control Table		
	SYS_LED_MASK#	LID_CL#
Mask All LEDs (Sniffer Function)	0	X
Mask Base MB LEDs (Lid Closed)	1	0
Do not Mask LEDs (Lid Opened)	1	1

Fiducial Mark

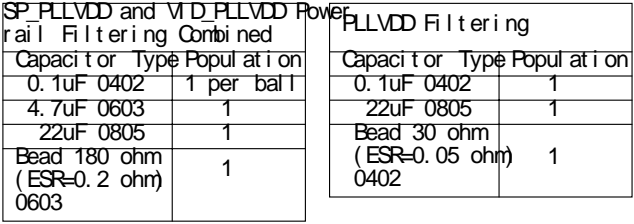


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I2CSlave Address

SMBUS_ALT_ADDR	Description
0	0x9E(Default)
1	0x9C(Multi - GPU usage)

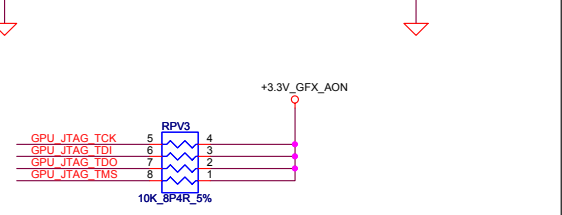
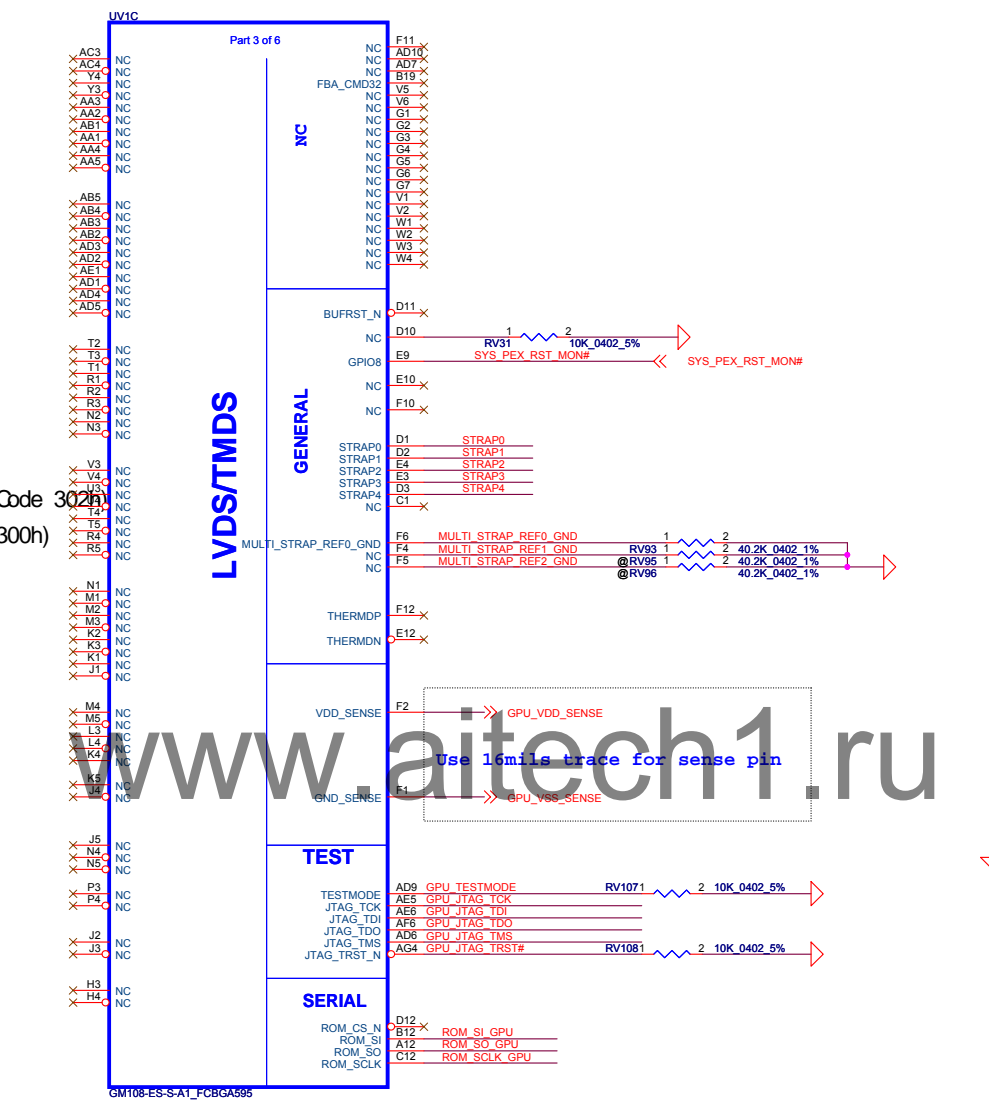
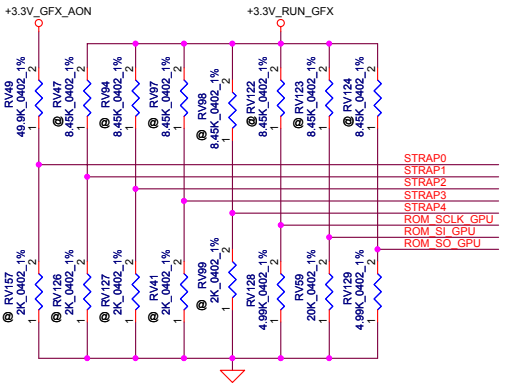
VGA_DEVICE Setting

VGA_DEVICE	Description
0	Non-Primary 3D Acceleration Device(Class Code 3020)
1	Primary Display or VGA Device(Class Code 300h)

Resistance Mapping to Hex Values

Resistor Value	Full-up to VDD3	Full-down to GND
4.99K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
24.9K	1100	0100
30.1K	1101	0101
34.8K	1110	0110
45.3K	1111	0111

Decide ID change to 0x1056



Strap Pin Name	Logical Strapping Bit 3	Logical Strapping Bit 2	Logical Strapping Bit 1	Logical Strapping Bit 0	Note
ROM_SCLK	SOR3_EXPOSED->0	SOR2_EXPOSED->0	SOR1_EXPOSED->0	SOR0_EXPOSED->0	ROM_SCLK pull-down 4.99k to GND
ROM_SI	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]	ROM_SI pull-down 20k to GND
ROM_SO	DEVID_SEL->0(default)	PCIE_CFG->0(default)	SMB_ALT_ADDR->0(default)	VGA_DEVICE->0	ROM_SO pull-down 4.99k to GND
STRAP0	Keep pull up to 3V3_AON and pull-down to GND footprint and stuff 50k ohm pull up				STRAP0 pull up 50k to +3.3V_GFX_AON
STRAP1 STRAP2 STRAP3 STRAP4	Reserve				

DEVID_SEL/PCIE_CFG default set 0, need refer Platform Update Notification for the latest configuration

VENDER	STRAP	Part Number	Note(ROM_SI)
Hynix	0x3	H5TC4G63AFR-11C	20k PD
Micron	0x4	MT41J256M16HA-093G.E	24.9k PD need change to MT41K256M16HA-107G.E
Samsung	0x5	K4W4G1646D-HC1A	30.1k PD

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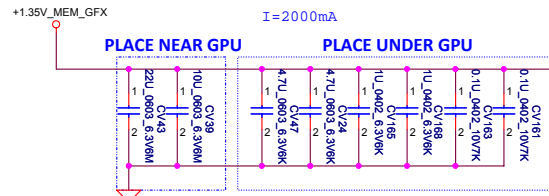
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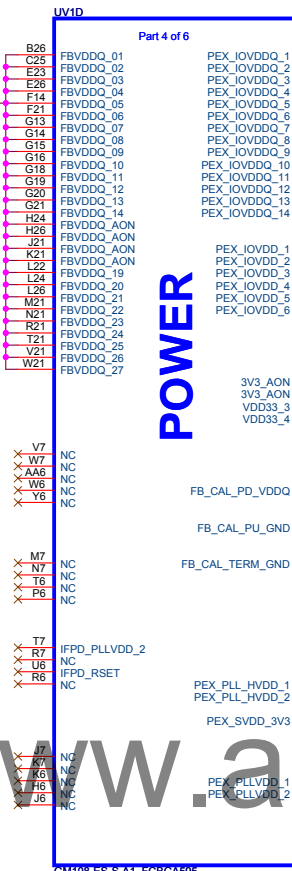
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DDR3 CPU side FBVDDQ/FBVDDQ2 Combined Decoupling		
Capacitor	Type	Population
0.1uF 0402		2
1.0uF 0603		2
4.7uF 0603		2
10uF 0805		1
22uF 0805		1

Power Supply Rail	N155-GM	N155-GT
	(V)	(A)
GPU Core	-	26
GPU FBIO	1.5 / 1.35	TBD
PEX_I/O VDDQ	1.05	0.765
PEX_PLLVDD	1.05	0.130
FBA_PLL_AVDD	1.05	0.062
FBA_DLL_AVDD	1.05	0.032
PLL_VDD	1.05	0.058
SP_PLLVDD	1.05	0.030
1.05V Total	1.05	1.060
VDD3+3V3AON	3.3	0.036
PEX_SVDD_3V3	3.3	0.167
PEX_PLL_HVDD	3.3	0.022
3.3V Total	3.3	0.225



PEX_PLLVDD Decoupling		
Capacitor	Type	Population
0.1uF 0402		1
1uF 0603		1
4.7uF 0805		1

PEX_SVDD/PEX_PLL_HVDD Decoupling		
Capacitor	Type	Population
0.1uF 0402		1
4.7uF 0603		2

3V3_MAIN Decoupling		
Capacitor	Type	Population
0.1uF 0402		2
1uF 0603		1
4.7uF 0603		1

3V3_AON Decoupling		
Capacitor	Type	Population
0.1uF 0402		1
1uF 0603		1
4.7uF 0603		1

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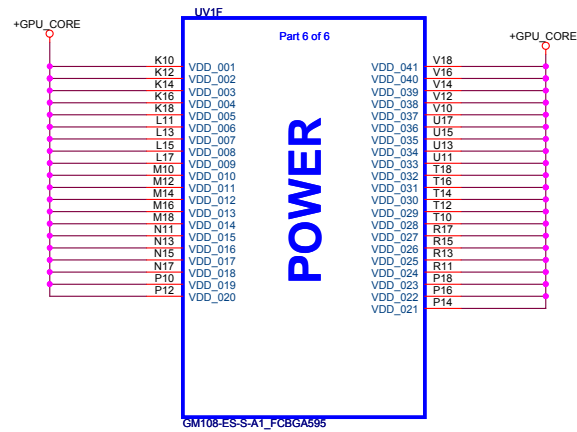
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Caps on Power Side
1UX4 4.7UX10 under GPU
4.7UX5 22UX1 47UX2 330UX2 near GPU



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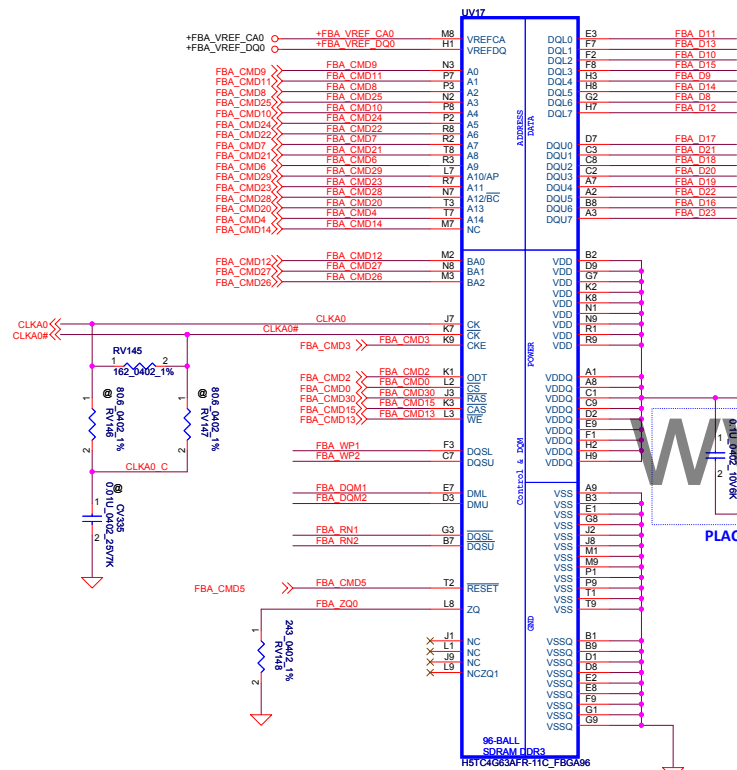
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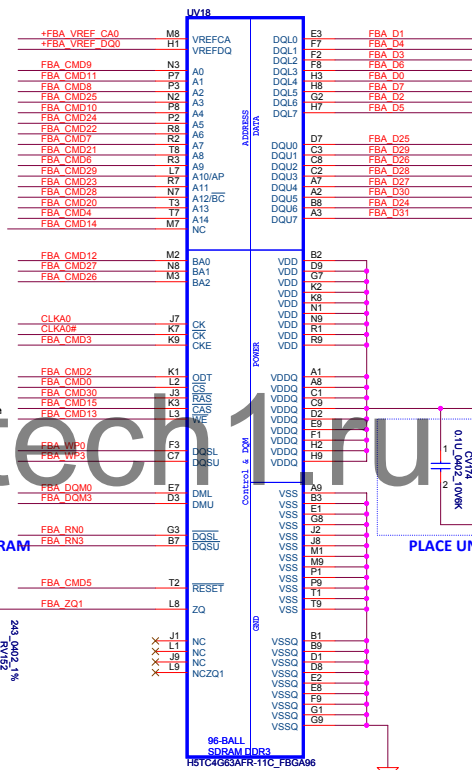
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FBA_DOM[0..3] <<>> FBA_DOM[0..3]
FBA_RN[0..3] <<>> FBA_RN[0..3]

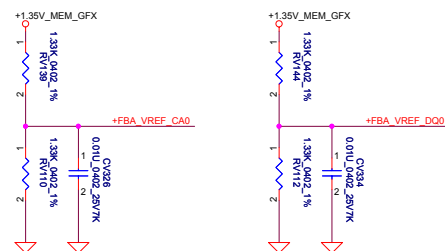


SA00006E800 Link done



SA00006E800 Link done

DDR3 per Memory FB/DD Q Decoupling		
FB/DD Q Combined		
Capacitor Type	Population	
0.1uF 0402	2	
1.0uF 0603	4	
10uF 0805	0	

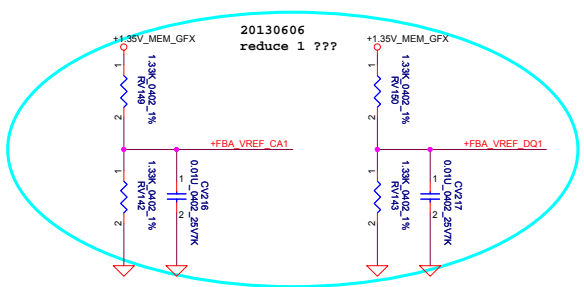
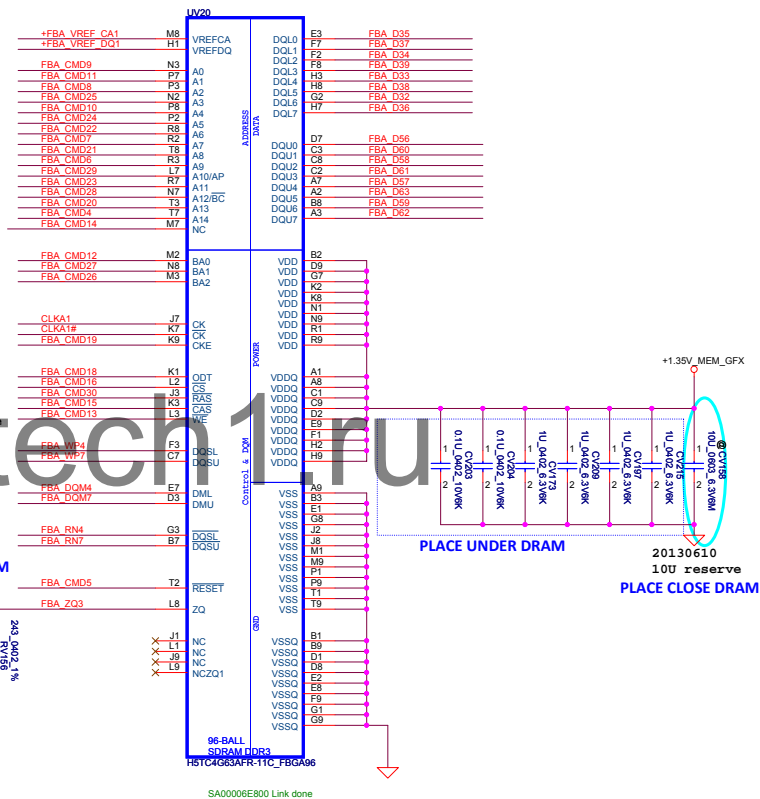
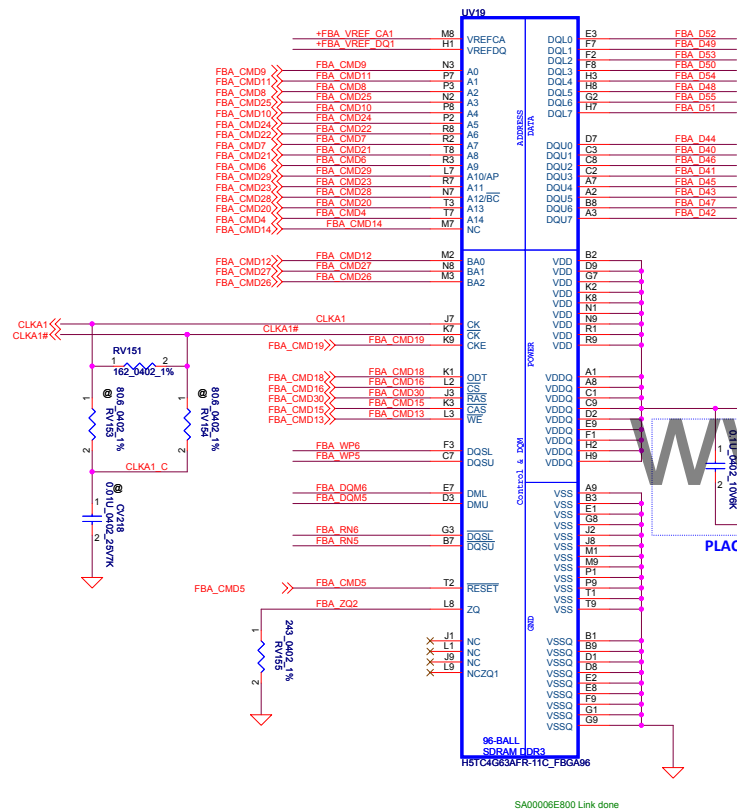


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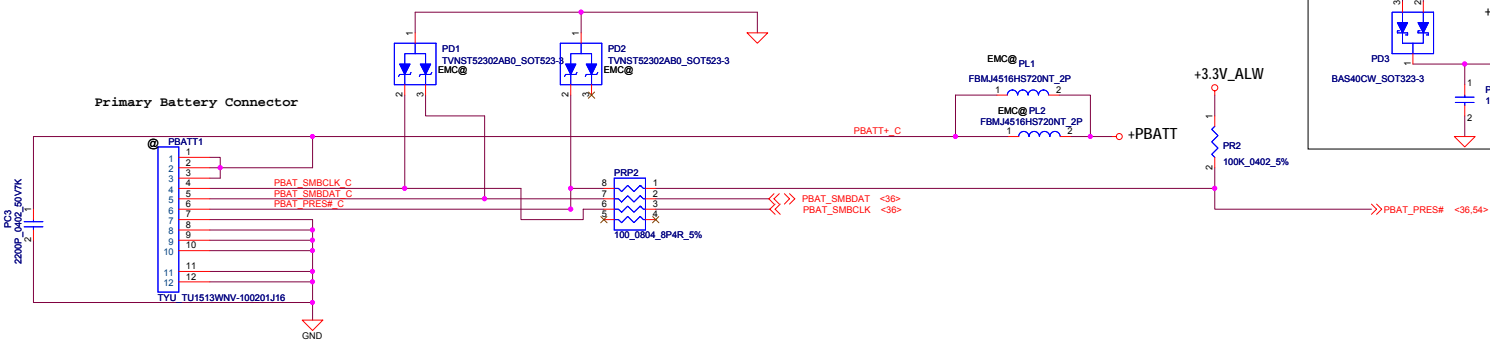
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FBA_RN[4..7] <<> FBA_RN[4..7]



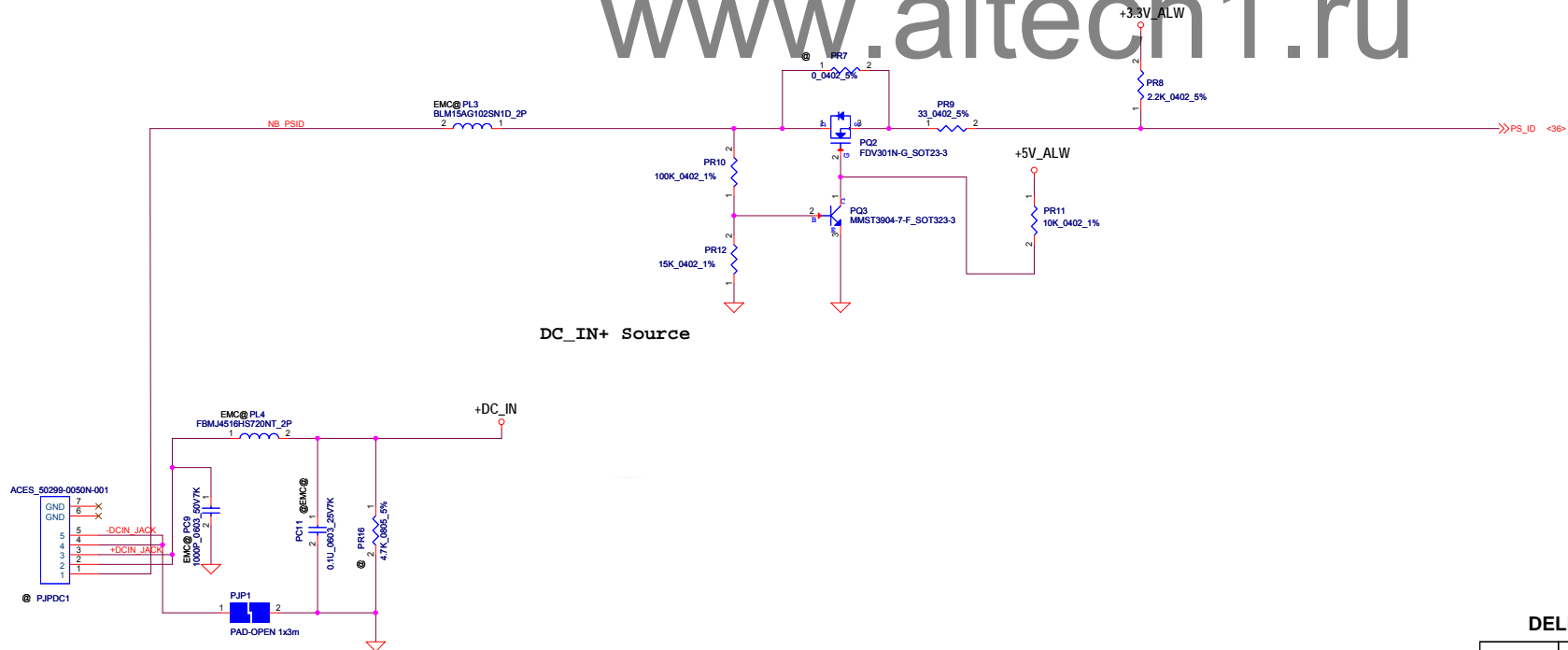
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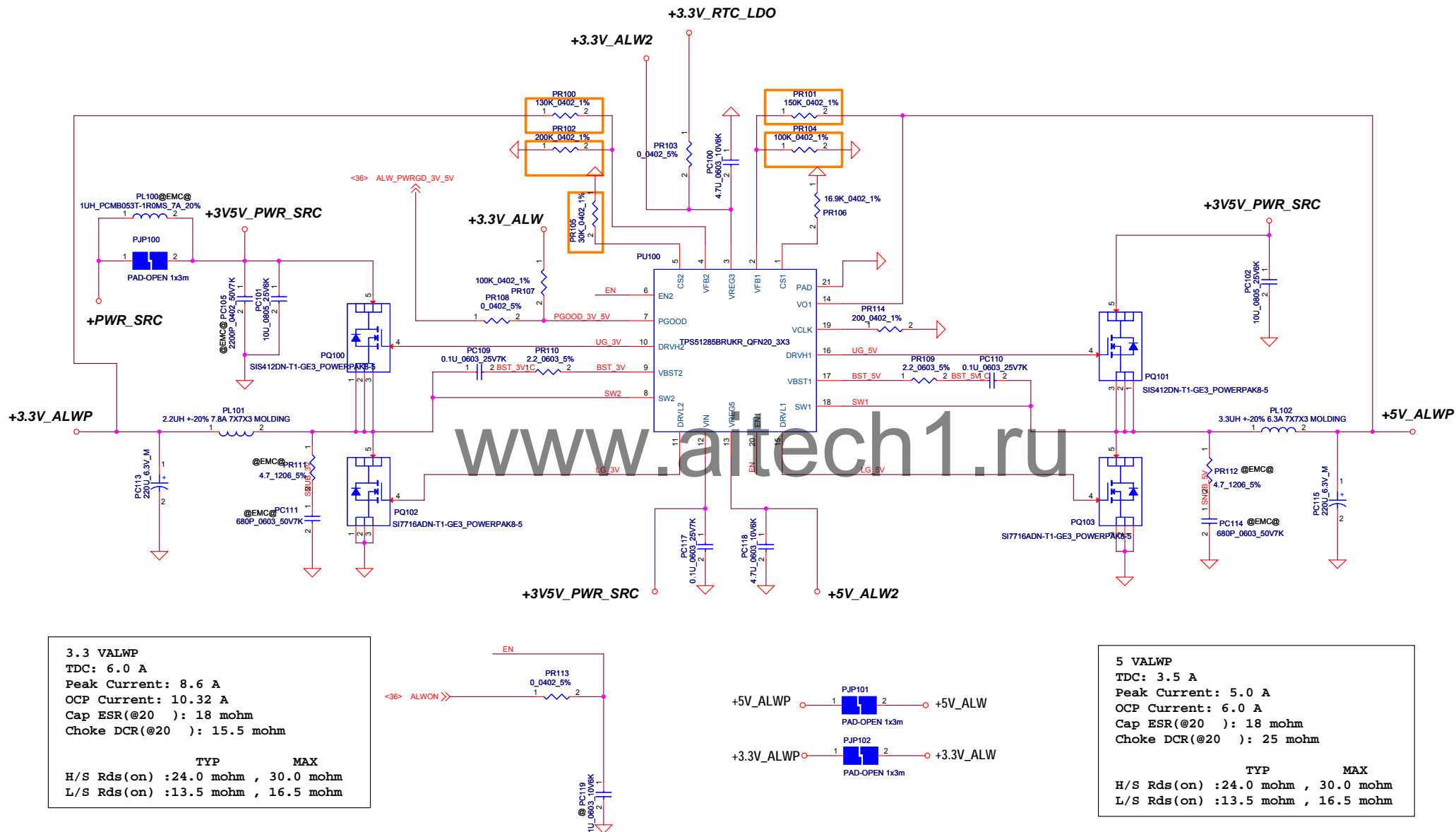
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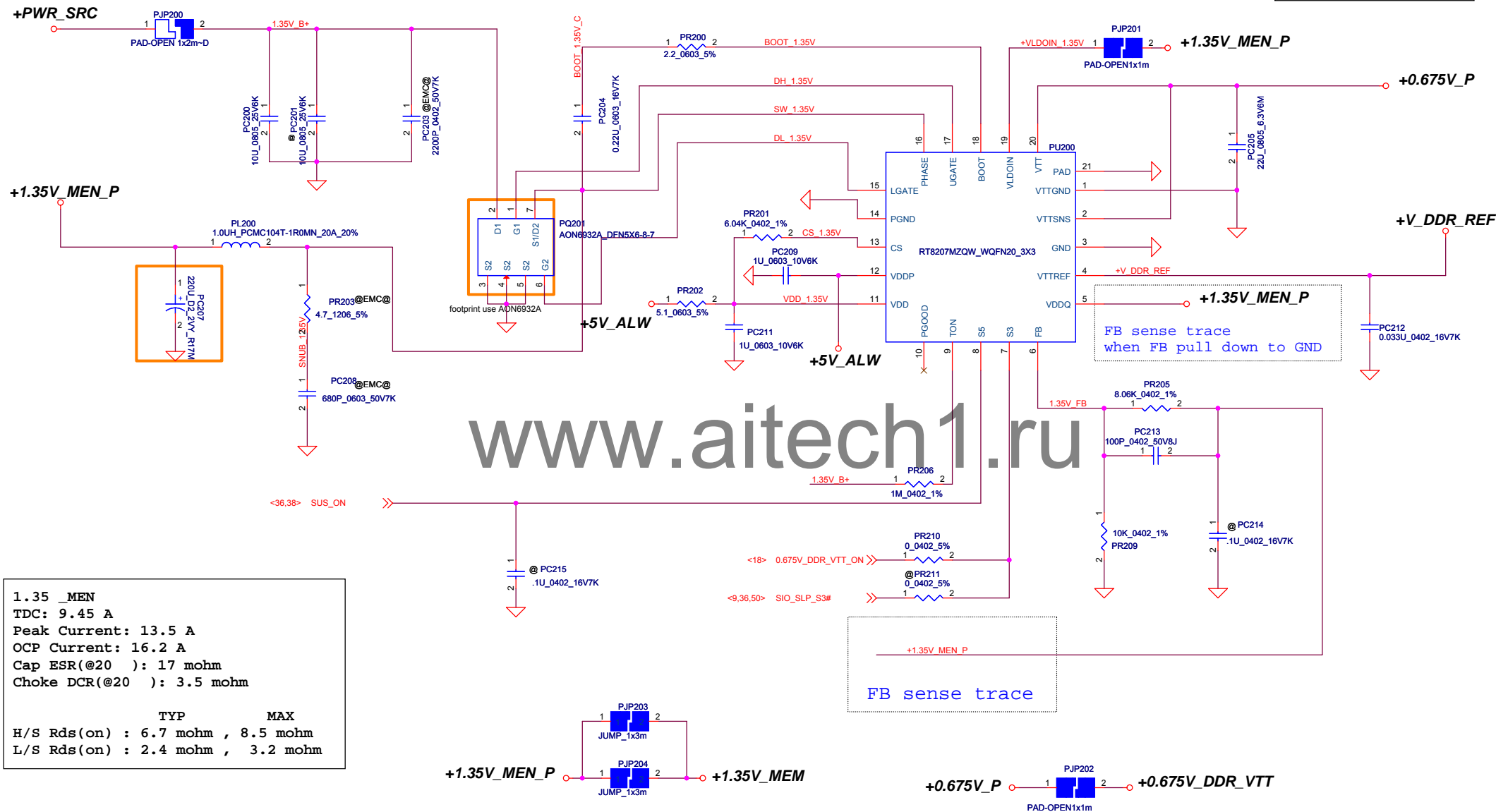
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0.675 Volt
TDC 0.7 A
Peak Current 1.0 A
OCP Current 1.2 A



1.35_MEN
TDC: 9.45 A
Peak Current: 13.5 A
OCP Current: 16.2 A
Cap ESR(@20): 17 mohm
Choke DCR(@20): 3.5 mohm

TYP MAX
H/S Rds(on) : 6.7 mohm , 8.5 mohm
L/S Rds(on) : 2.4 mohm , 3.2 mohm

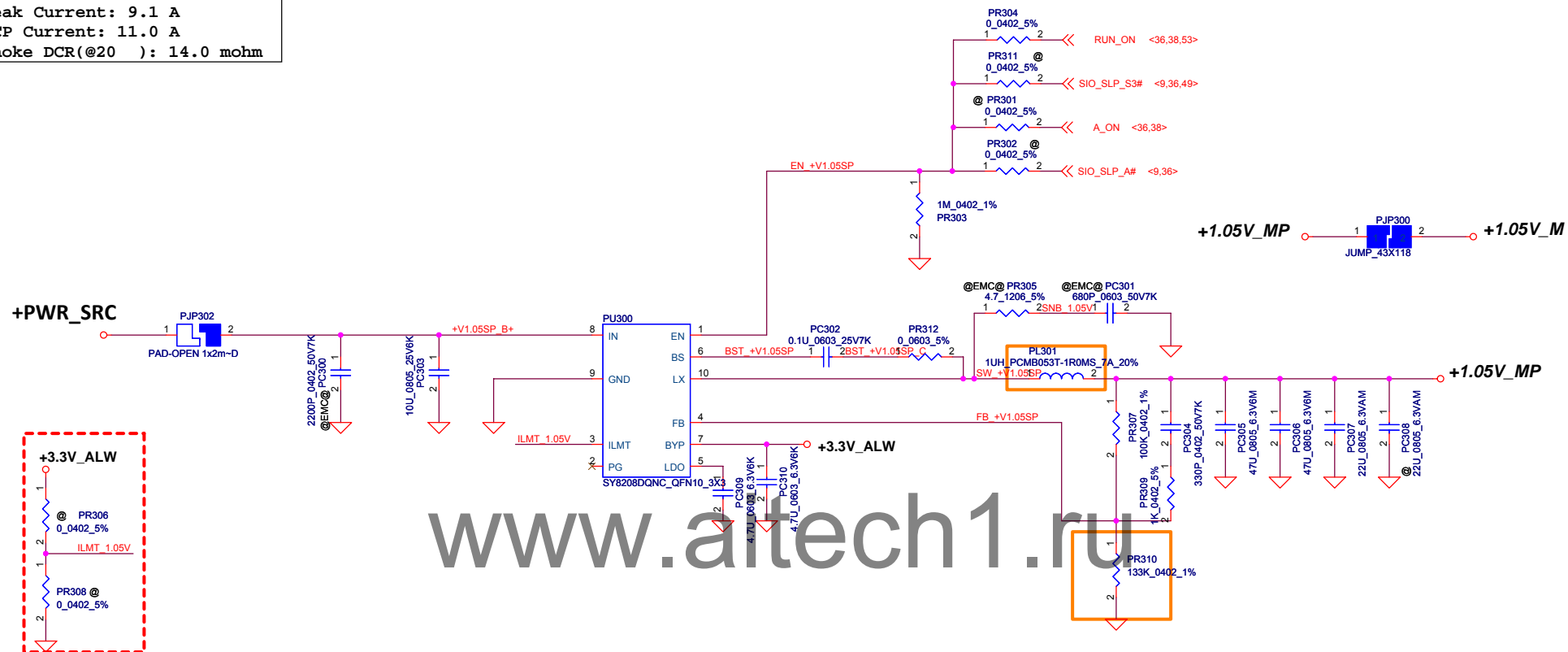
Mode	S3	S5	+1.35V_MEN	+V_DDR_REF	+0.675V_P
S5	L	L	off	off	off
S3	L	H	on	on	off (Hi-Z)
S0	H	H	on	on	on

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```
+1.05V_MEN
TDC: 6.5 A
Peak Current: 9.1 A
OCP Current: 11.0 A
Choke DCR(@20 ): 14.0 mohm
```



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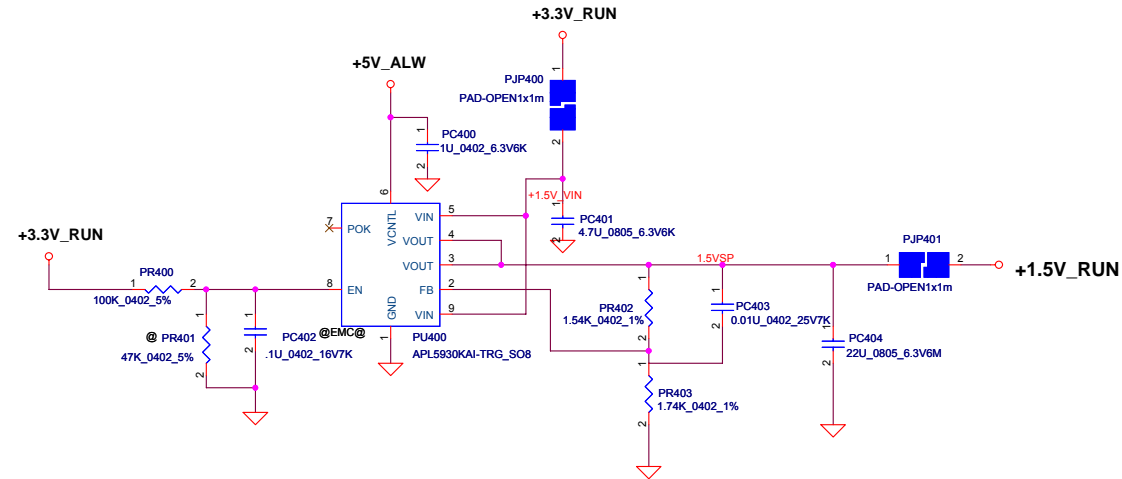
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+1.5V_RUN
TDC: 0.47 A
Peak Current: 0.67 A



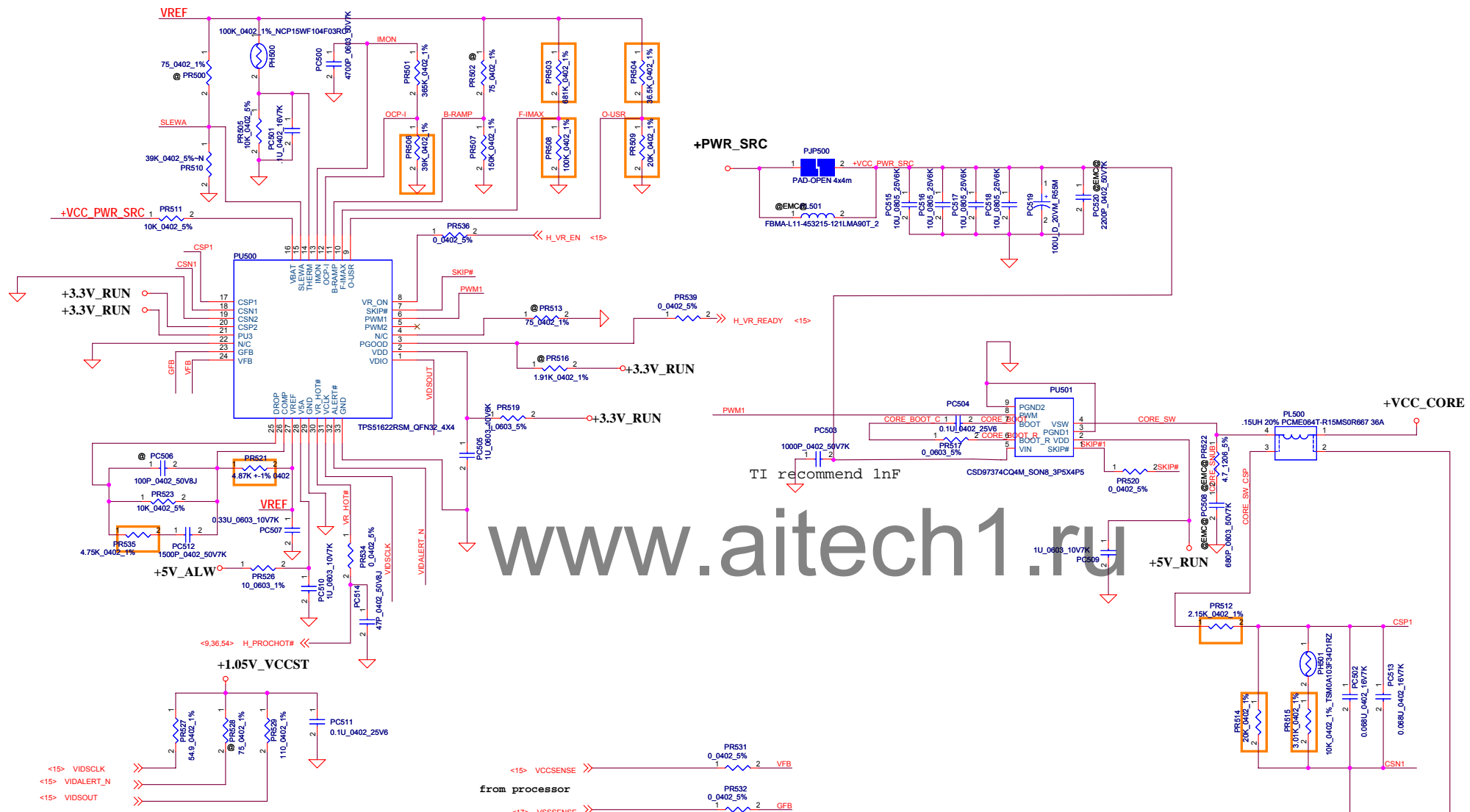
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CPU 15W
TDC 10 A
Peak Current 32 A
OCP Current 38.4 A
DC Load line -2.0 mV/A
Choke DCR: 0.66m +-7% ohm
Icc_Dyn_VID1 27 A
PH500 B value: 4250k 1%
PH501 B value: 3370k 1%

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Vboot=Vvref*(Rref1/(Rref1+Rf2+Rboot))
 Rt=Rrefadj // (Rboot+Rref2)
 $V_{min} = V_{vref} * [R_{ref2} / (R_{ref2} + R_{boot})] * [R_t / (R_{ref1} + R_t)]$
 $V_{max} = V_{vref} * R_{ref2} / [(R_{ref1} // R_{refadj}) + R_{boot} + R_{ref2}]$
 $V_{out} = V_{min} + N * V_{step}$
 $V_{step} = (V_{max} - V_{min}) / N_{max}$

PWM-VID Spec and component Values

PWM-VID Spec	Config A	Config B	Config C
Vmin	0.6V	0.6V	0.65V
Vmax	1.2V	1.2V	1.15V
Vboot	0.875V	0.9V	0.9V
Voltage step	6.25mV	6.25mV	25mV
N of Voltage level	96	96	20
Rrefadj	PR9	39K	20K
Rref1	PR5	39K	20K
Rboot	PR8	1.5K	2K
	PR10	30K	18K
Rref2=PR10+PR12	PR12	1.5K	0
C	PC8	1.5nf	2.7nf

Module model information:
 RT8813A_V1A for IC module
 RT8813A_V1B for SW module

Current Limit threshold setting
 $R_{ocset} = (I_{valley} * R_{ds(on)} + 40 \text{ mV}) / 10 \mu\text{A}$
 $I_{ripple} = (19 - 0.9) * 0.9 / (304.89 \text{ Khz} * 0.36 \mu\text{s} * 19) = 7.811 \text{ A}$
 $OCP = 54 \text{ A} / 2 = 27 \text{ A}$ per phase
 $I_{valley} = 27 \text{ A} * 7.811 \text{ A} / 2 = 23.1 \text{ A}$

H-side MOS:TPCA8065
 $R_{ds(on)} = 11.7 \text{ mohm} @ V_{gs} = 10 \text{ V}$
 $9.4 \text{ mohm} @ V_{gs} = 4.5 \text{ V}$
 $I_d = 16 \text{ A} @ T_a = 25 \text{ degC}$
 L-side MOS:TPCA8057
 $R_{ds(on)} = 2.0 \text{ mohm} @ V_{gs} = 10 \text{ V}$
 $2.6 - 3.2 \text{ mohm} @ V_{gs} = 4.5 \text{ V}$
 $I_d = 42 \text{ A} @ T_a = 25 \text{ degC}$

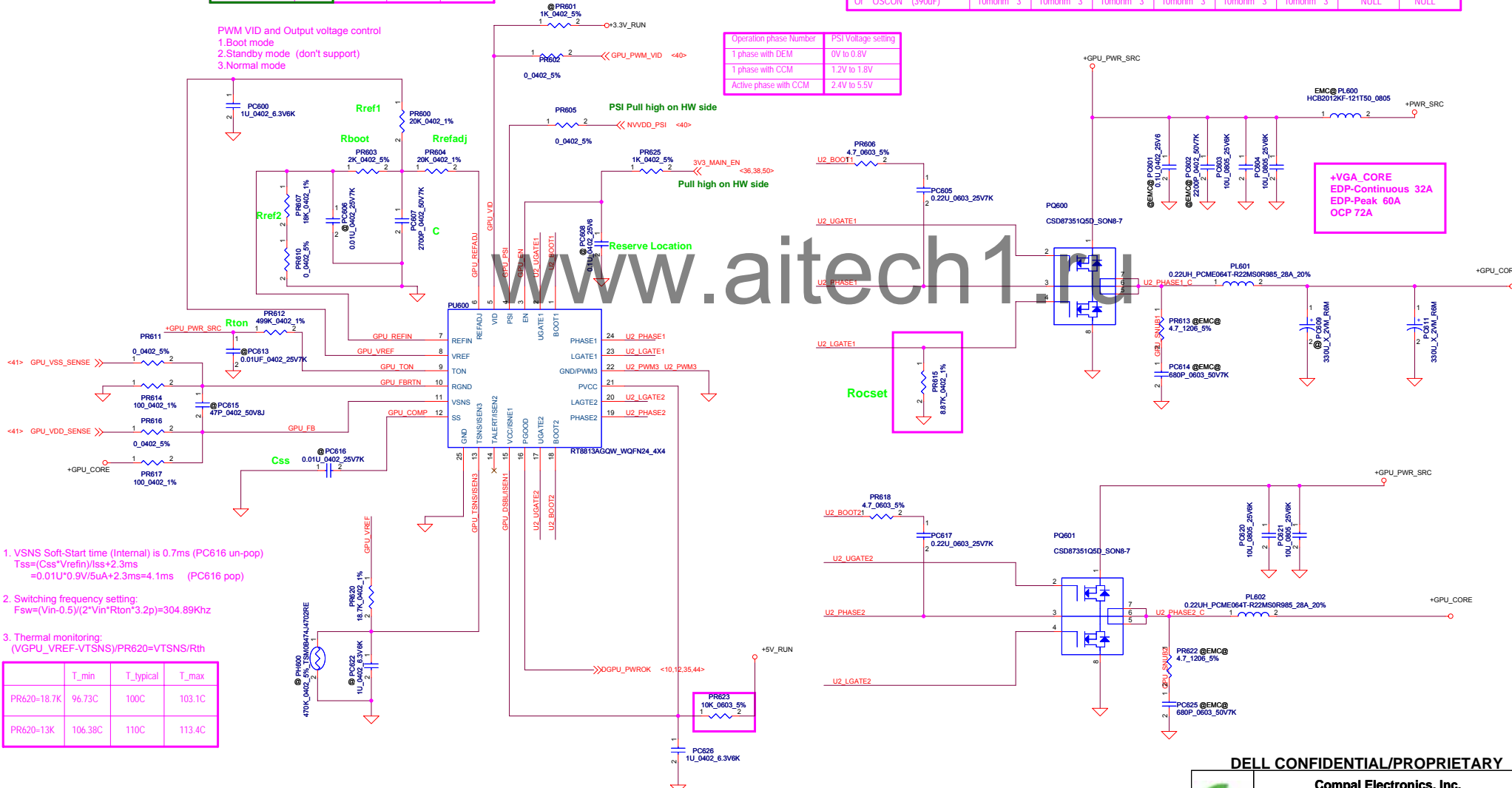
Choke: 0.36uH (Size:10*10*4)
 $R_{dc} = 1.1 \text{ mohm} \pm 5\%$
 Heat Rating Current=30A
 Saturation Current=50A

$C = 3 * 330 \mu\text{F} (9 \text{ mohm}) = 990 \mu\text{F}$
 $V_{ripple} = \text{ripple} * ESR(\text{min}) = 7.811 \text{ A} * 3 \text{ mohm} = 23.4 \text{ mV}$

Different VGA Chip (different EDP-Peak Current) need select different solution

VGA Chip	N14P-GV	N14P-GV2	N14M-GS	N14M-LP	N14P-LP	N14P-GE	N14P-GS	N14P-GT
OpenVReg Configurations	Config B	Config B	Config B	Config B	Config B	Config B	Config B	Config B
Rated TDP Power at Tj=102C	18W	25W	18W	13W	18.9W	25W	25.6W	35.5W
Boosted GPU Total at Tj=102C	25W	32W	25W	20W	23W	N/A	30W	40W
EDP-Continuous at Tj=102C	24A	32A	26A	22A	25A	27A	38A	45A
EDP-Peak at Tj=102C	35A	55A	45A	35A	35A	40A	60A	75A
Istep max (Evaluation)	15A	27A	25A	20A	14A	12A	31.5A	35A
OCP Setting Current	42A	66A	54A	42A	42A	48A	72A	90A
Rocset	8.96K	12.45K	10.7K	8.96K	8.96K	9.83K	8.3K	9.39K
Recommendation	2phase 1H1L	2phase 1H1L	2phase 1H1L	2phase 1H1L	2phase 1H1L	2phase 1H1L	2phase 1H2L	2phase 1H2L
Polymer Cap (330uF)	6mohm * 2	9mohm * 3	9mohm * 3	6mohm * 2	6mohm * 2	6mohm * 2	6mohm * 3 (L=0.22uH)	4.5mohm * 3 (L=0.15uH)
Or OSCON (390uF)	10mohm * 3	10mohm * 3	10mohm * 3	10mohm * 3	10mohm * 3	10mohm * 3	NULL	NULL

PWM VID and Output voltage control
 1.Boot mode
 2.Standby mode (don't support)
 3.Normal mode



- VSNS Soft-Start time (Internal) is 0.7ms (PC616 un-pop)
 $T_{ss} = (C_{ss} * V_{refin}) / I_{ss} + 2.3 \text{ ms}$
 $= 0.01 \mu\text{F} * 0.9 \text{ V} / 5 \mu\text{A} + 2.3 \text{ ms} = 4.1 \text{ ms}$ (PC616 pop)
- Switching frequency setting:
 $F_{sw} = (V_{in} - 0.5) / (2 * V_{in} * R_{ton} * 3.2 \text{ p}) = 304.89 \text{ Khz}$
- Thermal monitoring:
 $(V_{GPU_VREF} - V_{TSNS}) / PR620 = V_{TSNS} / R_{th}$

	T_min	T_typical	T_max
PR620=18.7K	96.73C	100C	103.1C
PR620=13K	106.38C	110C	113.4C

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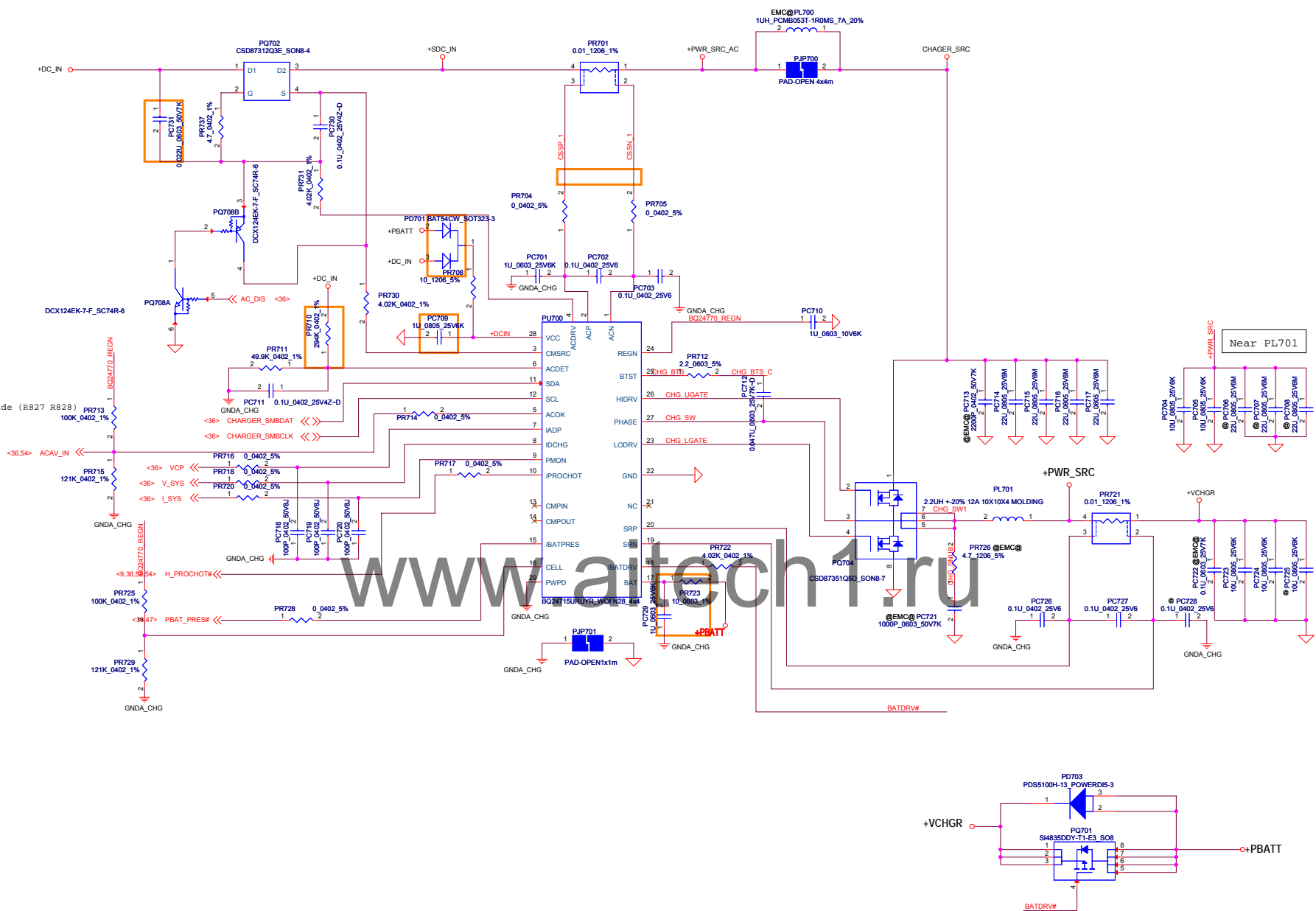
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
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CHARGER_SMBCLK
CHARGER_SMBDAT
pull up 10K in HW side (R827 R828)

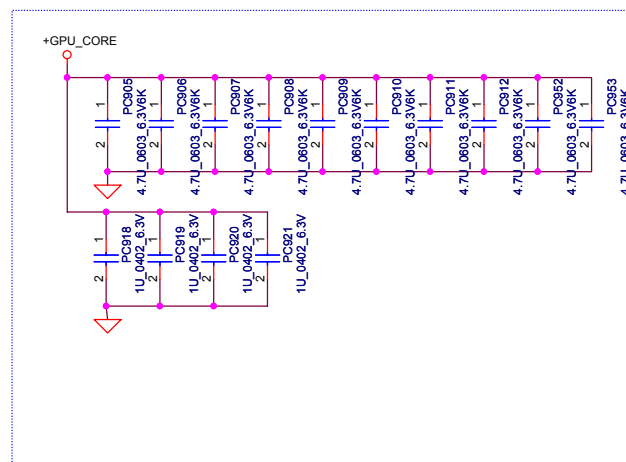
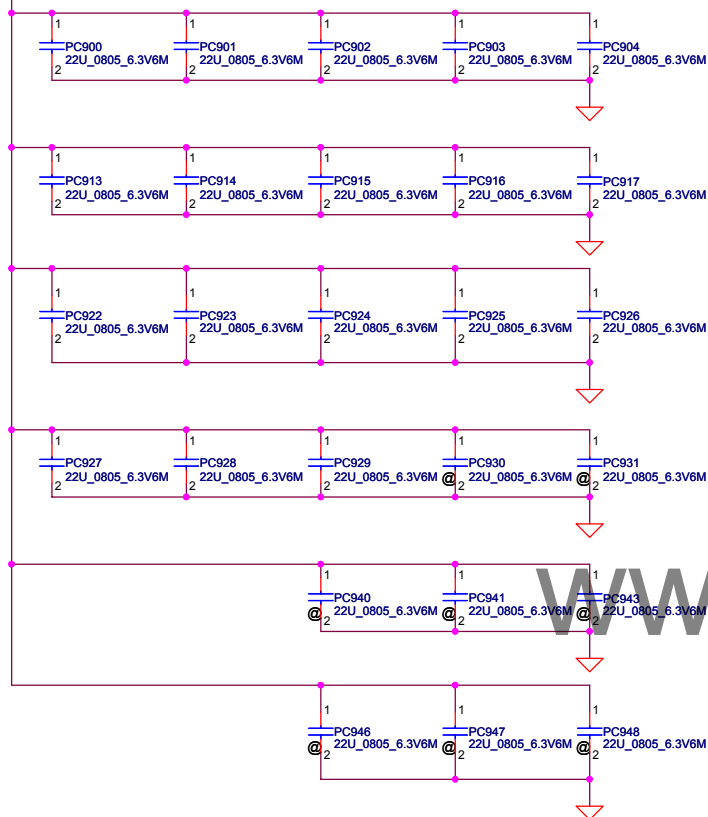


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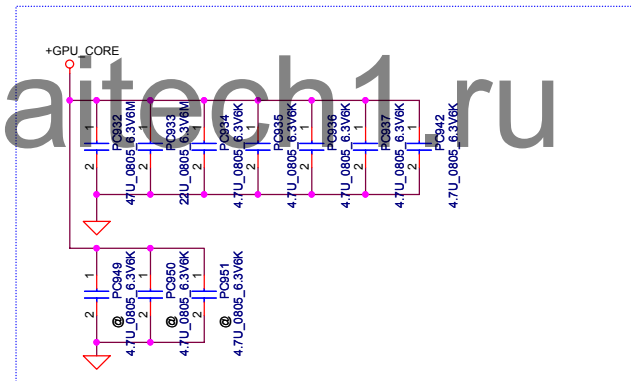
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+VCC_CORE



nVidia GB2B-64 package
Under GPU
4.7uF 0603 * 10
1uF 0402 * 4



nVidia GB2B-64 package
Near GPU
47uF 0805 *1
22uF 0805 *1
4.7uF 0805 *5

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